Graphene Field Effect Devices and Circuits - Theory and Fabrication

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PAR

Clemens Benedict NYFFELER

acceptée sur proposition du jury:

Dr G. Boero, président du jury
Prof. Y. Leblebici, directeur de thèse
Prof. J.-P. Leburton, rapporteur
Dr I. Shorubalko, rapporteur
Dr J.-M. Sallese, rapporteur

ÉCOLE POLYTECHNIQUE
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I have a thing for tools.
— Tim Allen

In memoriam
Simon "Peschmä" Rutishauser

Abstract

Electronics today permeate our life and existence. It has become nearly impossible to evade any dependence on electronic devices that surround us every day - computers, phones, televisions. But also other objects become increasingly "smart" - watches, cars, coffee machines, even entire buildings. Without necessarily being aware of it, every person in our modern world is the owner of billions, probably tens of billions of transistors. These elementary switches are the primitive units, of which all electronic devices are made, much like biological cells constitute our bodies.

Decades of technological progress at an incredible pace have been fueled by the constant improvement of semiconductor device technology. The original combination of silicon, silicon dioxide and aluminum required to build a transistor, has been complemented by a myriad of other materials. One of the last remainders of the original technology, the silicon channel, is now about to be replaced as well. While a short term remedy for the present performance bottleneck might be found in III-V compounds a more compelling alternative could be found in 2D materials.

Graphene was not only the first 2D material to be discovered and isolated in 2004, but also has the most extraordinary electric properties, owing to the high symmetry of its lattice. The content of this thesis presents a broad examination of the graphene field effect device reaching from the fabrication over electrical characterization to data analysis, device modeling and finally simulation of a small circuit.

In this thesis, we present practical considerations regarding the experimental examination of graphene field-effect devices. A fabrication flow tailored for top-gated graphene devices was developed, taking into account the particular requirements and sensitivities of the material. We also describe a set of versatile software tools that were developed for the design of devices, chips and wafers, their automated electric characterization and finally for browsing and visualizing the measurement results. The data analysis was performed with a very effective conductance-based model, which is based on semi-empirical models commonly used to describe graphene devices. We provide an overview of these models, the phenomena which they take into account and the steps that can be taken to improve their accuracy to obtain the model we finally utilized.

A environment was created to use our model in a SPICE-like circuit simulator in order to study possible topologies in which graphene devices could constitute an elementary circuit block.

Abstract

We focus our study on devices that operate as a differential pair, resembling the configuration that also enables very high-speed source-coupled and emitter-coupled logic circuits based on standard silicon transistors. Using analytical calculations we determine tuning parameters and their optimum values to maximize the transfer characteristics of our graphene-based differential circuit block.

In order to achieve more accurate simulation and as a means to verify the empirical model, we worked on a more rigorous approach. Based on first principles, we construct a model building on the specific carrier statistics in graphene. These deviate from the usual Boltzmann statistics and lead to a an equation describing the device's charge-voltage relation, which is transcendental and cannot ordinarily be solved. By using asymptotic approximations, we obtain closed-form expressions for the device current as a function of bias conditions. Unlike many other models, we can discriminate both between electron and hole currents as well as between drift and diffusion currents, making the model well-suited for implementation as a compact model.

Keywords: graphene, circuit, transistor, differential logic, fabrication process, characterization, modeling, simulation

Zusammenfassung

Elektronik durchdringt heute unser Leben und unsere Existenz. Kaum jemand kann sich der Abhängigkeit der elektronischen Geräte entziehen, die uns tagtäglich umgeben – Computer, Mobiltelefone, Fernseher. Aber auch andere Objekte werden immer mehr durch ßmarte"Gegenstücke ersetzt, wie etwa Armbanduhren, Autos, Küchengeräte, ja sogar ganze Gebäude. In unserer modernen Gesellschaft ist fast jeder im Besitz von wohl duzenden milliarden Transistoren, ohne sich dessen zwangsläufig bewusst zu sein. Diese fundamentalen Schaltelemente liegen allen elektronischen Geräten zugrunde, ähnlich wie alles Leben sich aus biologischen Zellen zusammensetzt.

Angetrieben durch andaurnde Verbesserung der Halbleiterherstellungstechnologie haben wir Jahrzente technologischen Fortschritts in einem unglaublichen Tempo erlebt. Zu der ursprünglichen Kombination aus Silizium, Siliziumdioxid und Aluminium, mit der Transistoren anfangs gebaut wurden, ist mittlerweile eine Unzahl anderer Materialien dazugekommen. Einer der letzen Bestandteile der urspünglichen Technologie, der Silizium-*Channel*, soll nun ebenfalls ersetzt werden um den nächsten Leistungsengpass zu überwinden. Kurfristig werden hier wohl III-V-Verbindungen Abhilfe schaffen, doch längerfristig könnten 2D-Materialien eine interessantere Alternative bieten.

Graphen ist nicht nur das erste 2D-Material, das im Jahr 2004 entdeckt wurde, es hat angesichts der besonderen Gittersymmetrie auch die aussergewönlichsten Eigenschaften. Der Inhalt dieser Dissertation beschreibt eine breite Auseinandersetzung mit dem Graphen-Feldeffektdevices und reicht von Herstellung und Fabrikation über eletkrische Characterisierung hin zu Datenanalyse, Modellierung und schliesslich zur Simulation eines einfachen Schaltkreises.

In der vorliegenden Arbeit, präsentieren wir eine praktische Auseinandersetzung mit der experimentellen Untersuchung des Graphen-Feldeffektdevices. Zunächst wurde ein Fabrikationsprozess erarbeitet, der auf die spezifischen Anforderungnen in Bezug auf Graphen und die Empfindlichkeit des Materials besondere Rücksicht nimmt. Wir berichten ferner über eine Reihe vielseitiger Software-Tools, die für die Verschiedenen Arbeitsphasen entwickelt wurden, insbesondere für das Layoutdesign von Devices, Chips und Wafers, dann deren automatisierte elektrische Charakterisierung und schliesslich für das Verzeichnen, Durchsuchen und Visualisieren der Messresultate. Die Datenanalyse wurde mittels eines äusserst effektiven, Konduktanzbasierten Modells durchgeführt, welches auf bestehenden semi-empirischen Modellen aufbaut, die gewöhnlich zur Beschreibung von Graphen-Devices verwendet werden.

Wir liefern eine Übersicht über diese Modelle, die Eigenschaften und Phänomene die sie berücksichtiguen sowie Änderungen, anhand derer ihre Genauigkeit verbessert werden kann.

Eine Entwicklungsumgebung wurde erstellt, mit der wir unser Modell in einem SPICE-ähnlichen Schaltungssimulator verwenden können, um mögliche Topologien zu untersuchen, anhand derer mit Graphen-Devices ein ein elementarer Schaltungsblock gebildet werden könnte. Wir konzentrierten uns dabei auf eine Schaltung, die ähnlich wie ein Differenzverstärker funktioniert und sich an das Prinzip der *Source Coupled Logic*- bzw *Emitter Coupled Logic*-Hochgeschwindigkeitsschaltungen anlehnt. Anhand analytischer Berenchnungen haben wir Parameter bestimmt und deren Werte optimiert, um die Übertragungscharakteristik unseres differenziellen Schaltungsblocks zu maximieren.

Um einerseits noch präzisere Simulationen zu ermöglichen und andererseits unser empirisches Modell zu verifizieren, haben wir ein weiteres, auf den Grundprinzipien basiertes Modell erarbeitet. Die besondere Ladungsträgerstatistik in Graphen, die sich von der sonst üblichen Boltzmannverteilung unterscheidet, führt zu einer transzendenten Beziehung zwischen Ladung und Spannung die im Prinzip nicht analytisch lösbar ist. Wir verwenden hier asymptotische Näherungen um dennoch Lösungen für den Stromfluss im Graphen-Device in geschlossener Form zu erhalten. Im Gegensatz zu anderen Modellen können wir sowohl zwischen Elektronen- und Löcherstrom als auch zwischen Drift- und Diffusionsstrom unterscheiden. Das Modell eignet sich überdies auch zur Implementierung als Kompaktmodell für Schaltungssimulationen.

Contents

1 Introduction

1.1 History

The ground-breaking research by the Manchester group[1], published in 2004 of is generally viewed as the starting point of the enduring surge in graphene research. The history of this new material, however, begins earlier with efforts to understand the electronic properties of graphite by Wallace in 1947[2] followed by by McClure and Slonczewski [3, 4] later in the 1950's. In all of these papers, the band structure of graphite is studied by calculating individual, two-dimensional graphite sheets.

The name *Graphene* was not coined until 1994 when it was made official by IUPAC[1] recommendations [5] out of need for a terminology in the field of graphite intercalation compounds. The use of the terms "graphite layer" or "carbon sheet" were deemed incorrect or inappropriate and so the suffix *"ene"*, that had been used for so-called fused polycyclic aromatic hydrocarbons, was adopted.

While more theoretical studies of graphene were made in 80's and 90's, these were generally viewed as pure academic exercises since the material was considered to be thermodynamically unstable and impossible to realize [6]. Despite these predictions, which may still strictly be valid for perfectly flat crystals, it appears graphene can exist due to the strong sp^2 bonding between its atoms and more importantly because of slight corrugations, on the order of a few nanometers, that were observed in 2007[7].

Since 2004, and in particular after the Nobel Price was awarded to Geim and Novoselov in 2010, there has been tremendous research interest. The number of graphene-related publications has exceeded 10 000 per year at the time of writing of this thesis.

1.2 Structure

Graphene consists of a single (one atom thick) layer of carbon atoms, arranged in a honeycomb lattice, making it a truly two-dimensional material, closely related to fullerenes, carbon nanotubes and graphite. The latter, familiar to all of us from writing with pencils, consists

[1] International Union of Pure and Applied Chemistry (iupac.org)

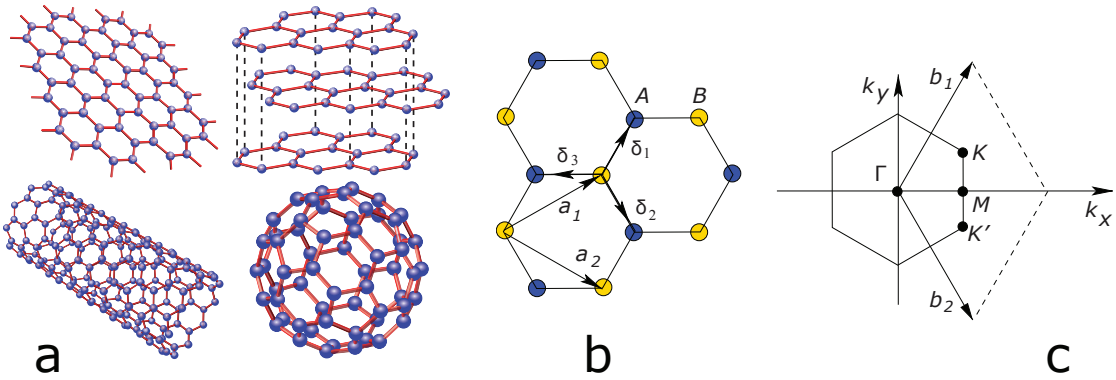


Figure 1.1 – Structure of Graphene: Graphene (top left) and similar allotropes of carbon: graphite, a fullerene and a carbon nanotube (clockwise) (a) Lattice structure of graphene in real space (b) and in reciprocal space (c). The lattice vectors have a length $a = 2.46$Å. The nearest neighbor distance is $\delta = a/\sqrt{3} = 1.42$Å. Images reprinted with permission from [9].

of layers of graphene stacked upon each other and weakly held together by *Van der Waals* forces. This weak binding between layers is responsible for the ease of creating marks by abrasion of the pencil's "lead" on the one hand, but also for the possibility of removing single layers by mechanical exfoliation (the "scotch tape method"). Contrarily to the weak inter-layer coupling, the intra-layer bonds are very strong: the atoms in graphene are connected by 1.42 Å sp^2 bonds, giving it its hexagonal structure and making it to date the strongest material ever measured[8].

Figure 1.1b illustrates the lattice structure of graphene, with its two unit vectors a_1, a_2 and the nearest-neighbor vectors $\delta_1, \delta_2, \delta_3$. It is noteworthy that these two unit vectors cannot span the entire hexagonal lattice of graphene, but only one of its two triangular sublattices A and B, which are represented by the blue and yellow circles, respectively. These sublattices are Bravais lattices whereas the honeycomb structure in itself is not. This is reflected in reciprocal space (figure 1.1b), with the two non-equivalent corner points K and K' of the Brillouin zone.

1.3 Band Structure

The special electronic properties of graphene derive from its unusual band structure and the absence of a band gap. An analytic expression can be obtained with a tight-binding approach, where only nearest neighbors are takin into account [2, 9]. The parameter $\gamma \approx 2.8$ eV is the nearest-neighbor hopping amplitude and a is the lattice constant:

$$E = \pm\gamma\sqrt{1 + 4\cos^2(k_y a) + 4\cos(k_y a)\cos(k_x\sqrt{3}a)} \tag{1.1}$$

Figure 1.2 shows a plot of equation (1.1), where the lower and upper surfaces are the conduction and valence bands, respectively. Intrinsic, isolated graphene in the ground state ($T = 0K$) has lower band completely filled with electrons and the upper band completely empty.

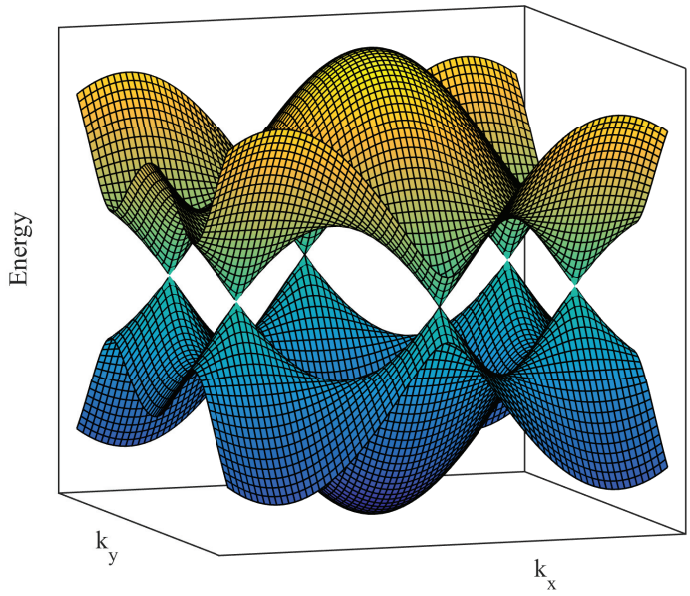


Figure 1.2 – Band structure as obtained by tight binding calculation.

The six points where the two surfaces touch correspond to the edges of the Brillouin zone and are called *K*-points or *Dirac*-points. The dispersion relation in the vicinity of these points has the shape of a double cone and can be expressed as $|E - E_D| \approx v_F|\vec{k} - \vec{k_D}|$, where E_D and $\vec{k_D}$ are energy and wavevector, respectively, at the Dirac point and $v_F \approx 10^6$m/s is the Fermi velocity. In other words, the dispersion relation is linear in graphene contrarily to the usual parabolic dependence found in semiconductors.

In a semi-classical description of semiconductors, the effective mass of an electron is often defined by means of the band curvature around the valence band minimum (conduction band maximum for holes). This approach does not work in the case of graphene, but it is reasonable to assume that the different nature of its band structure leads to a very different electron mass. In fact, it has been experimentally observed [10] and theoretically predicted [11] that carriers behave like so-called massless Dirac fermions in graphene: computing the tight-binding Hamiltonian of low-energy electrons near a K-point leads to an equation which is equivalent to the two-dimensional Dirac equation[2] with no mass term [9]. These discoveries are at the origin of the names *Dirac point* and *Dirac fermions*.

Since low effective mass is generally associated with high carrier mobility [12], extraordinarily high values of mobility can be expected in graphene.

[2]The Dirac equation, formulated by *Paul Dirac* in 1928 in an effort to reconcile quantum mechanics and special relativity, combines the Schrödinger Equation with the relativistic energy-momentum relation (a generalization of Eintein's famous $E = mc^2$) in order to explain the behavior of relativistically moving electrons.

1.4 Properties

Aside from being the first 2D material to be isolated and experimentally studied, the excitement graphene has brought into the scientific community also stems from the record-breaking mechanical and electronic properties it exhibits.

1.4.1 Carrier Mobility

Carrier mobility is probably the most important reason for the high interest in graphene among the electron device community, especially in light of the difficulties of further down-scaling transistors in current CMOS technology. One way to increase performance, other than shrinking transistor sizes, is boosting the channel material's mobility, which has a direct proportional impact on the transistor's on-current. This has been done in the past through strain engineering in Silicon but to achieve even higher mobility, the channel material has to be replaced entirely.

Mobility characterizes how charge carriers respond to an electric field inside a semiconductor in the diffusive transport regime, i.e. as long as the carrier's mean free path is smaller than the considered length of transport (e.g. the gate length in a transistor). In this case the carrier drift velocity is proportional to the applied electric field and the proportionality constant is the mobility: $\vec{v}_{\text{drift}} = \mu\vec{E}$.

The unit of mobility is *velocity* divided by *electric field* is usually expressed as cm^2/Vs:

$$[\mu] = \frac{\text{m/s}}{\text{V/m}} = \frac{\text{m}^2}{\text{Vs}} = 10^4 \frac{\text{cm}^2}{\text{Vs}} \tag{1.2}$$

Table 1.1 summarizes mobility values reported in the literature. The highest measured values of over $200\,000\,\text{cm}^2/\text{Vs}$ require cryogenic temperatures. With the use of hexagonal Boron-Nitride as a substrate, an electrically insulating 2D material with a structure very similar to graphene, mobilities even higher than in suspended graphene could be achieved. Even the smaller numbers in table 1.1 compare favorably to the state-of-the-art in high-mobility technologies such as InP ($15\,000\,\text{cm}^2/\text{Vs}$), InAs ($13\,200\,\text{cm}^2/\text{Vs}$) or strained Silicon ($1400\,\text{cm}^2/\text{Vs}$) [13].

Mobility is generally a constant under low-field conditions, but in modern transistors carrier velocities tend to saturate in certain conditions, e.g. when the electric field strength becomes larger than a critical value E_{crit}. The constant mobility is then usually replaced by a field-dependent *effective* mobility:

$$\mu_{\text{eff}} = \frac{\mu}{1 + \frac{E}{E_{\text{crit}}}} \tag{1.3}$$

More generally, mobilities are functions of various parameters, such as temperature or dopant concentration, and can be attributed to different scattering mechanisms. The overall resulting

cryogenic temperature		room temperature	substrate	reference
suspended	non-suspended			
		10 000	SiO_2	Novoselov 2004 [1]
		5000	SiO_2	Lemme 2008 [14]
230 000 (5 K)	25 000 (5 K)		SiO_2	Bolotin 2008 [15]
120 000 (100 K)	20 000 (100 K)	9000	SiO_2	Bolotin 2008 [15]
		10 000	hBN	Meric 2010 [16]
	80 000 (2 K)		hBN	Dean 2010 [17]
		1500	SiC	Lin 2010 [18]
1 000 000 (5 K)			n/a	Castro 2010 [19]
	275 000 (4 K)	125 000	hBN	Zomer 2011 [20]
	500 000 (50 K)	100 000	hBN	Mayorov 2011 [21]
		5000	Quartz	Ramon 2012 [22]
		8700	SiC	Guo 2013 [23]

Table 1.1 – Selected mobility measurements in graphene reported in the literature in chronological order. All mobility values are in cm^2/Vs

effective mobility is then dominated by the lowest one, according to Mathiessen's rule:

$$\frac{1}{\mu_{\text{eff}}} = \sum_i \frac{1}{\mu_i}. \tag{1.4}$$

The important scattering sources in graphene on SiO_2 were found to be charged impurities and remote optical phonons originating in the substrate[24]. In suspended graphene, mobility is also limited by impurities, albeit at lower concentration, and by acoustic phonons [25].

1.4.2 Electrical Conductivity

Conductivity is tightly linked with mobility but is also dependent on carrier concentration. In a mixed-carrier material with electron and hole concentrations n and p, mobilities μ_n and μ_p and q being the elementary charge, the conductivity is given by:

$$\sigma = qn\mu_n + qp\mu_p \tag{1.5}$$

The picture changes of course, when very small devices and/or low Temperatures are considered so that the mean free path of the charge carriers become comparable or smaller than, e.g. the gate length of a transistor. In these cases the carrier mobility is no longer a useful concept and other tools, such as the Landauer formalism, have to be applied.

Although carrier concentrations are expected to completely vanish at the Dirac point, where the density of states is zero, it was found early on by Novoselov, Geim et al. that a constant minimum conductivity of about 155 µS is always present regardless of measured mobility [10]. This minimum conductivity, quite precisely corresponds to $4q^2/h$, where the factor 4 multi-

plying the conductance quantum q^2/h is straightforwardly attributable to the two-fold spin and valley degeneracy. A more fundamental lower limit of conductivity, $4q^2/\pi h$ (49.31 µS), was later derived analytically from the Dirac equation [26] and has been experimentally confirmed [27]. This value was obtained by taking ballistic transport into account, while the larger value previously found was determined to be the limit in case of diffusive transport.

These results are significant with regards to graphene based electronic devices, since one immediate consequence is that any on-off current ratio will be fundamentally limited by the minimum conductance.

1.4.3 Mechanical Strength

According to the authors of a study carried out in 2008[8], graphene is the strongest material ever measured. They used nanoindentation by atomic force microscopy (AFM) on highly defect-free graphene sheets, suspended over a circular cavity, in order to determine it's elasticity and the amount of pressure necessary to break it. The former is expressed by Young's modulus, which was determined to be 1 Tera-Pascal (1.0 TPa); the latter, graphene's breaking strength, was found to be 40 N/m. This means that graphene could sustain reversible elastic deformations by over 20% [28] without rupture.

1.5 Synthesis

There exists today a variety of methods for producing graphene with varying quality, cost and scalability. Mechanical exfoliation[1] using a scotch-tape to peel off layers from highly ordered pyrolytic Graphite (HOPG) was originally used by the Manchester Group, and still today produces the best quality graphene samples. It is, however, hardly a repeatable process and randomly produces single-, bi- and few-layer Graphene flakes no more than a few microns large.

A large area alternative is the epitaxial growth of Graphene on SiC wafers [29]. This method is based on the thermal decomposition of the substrate material, which occurs at temperatures between 1200°C and 1800°C when Si atoms desorb from the surface.

A growth method based on chemical vapor deposition (CVD) on copper foils appears to be the currently most popular method of producing graphene. It is less costly than epitaxial graphene (due to expensive SiC wafers) yet allows for synthesis of large area graphene sheets [30]. In this process, carbon atoms originating from a methane gas flow at temperatures around 1000°C are adsorbed on the Cu surface in a self-limiting process [31]. To make the Graphene suitable for electronic device fabrication it has to be released from the Copper foil and transferred onto an insulating substrate, which is commonly a Silicon wafer covered by a layer of SiO_2.

1.6 Other 2D materials

The discovery of graphene laid the foundation not only for graphene-specific research. It started an entire new field in materials science centered on two-dimensional materials and its

applications.

A variety of existing bulk materials resemble graphite in its layered structure, where *van der Waals* or other weak forces such as hydrogen bonds hold together atomically thin sheets [32]. With advances in exfoliation and CVD techniques a large number of monolayer materials have been isolated from such layered materials and even more have been studied theoretically and may soon be experimentally realized as well [33]. While some of these resemble graphene in structure and electronic properties, there is a rich variety of 2D materials ranging from metallic, over semiconducting to isolating [33].

Closely related to graphene are silicene[34], germanene[35], phosphorene[3] [36] and most recently stanene[37, 38]. These are 2D materials arranged in a hexagonal lattice consisting of atoms of a single group IV (Si, Ge, Sn) or group V (P) element. With the exception of phosphorene, they are gapless, have the same cone-like band structure (which is commonly called the *Dirac cone*) and are expected to possess massles Dirac fermions and similar electronic properties as graphene [39]. Phosphorene on the other hand is a semiconductor with a predicted band gap of 1.0 eV [40]; initial experiments on few-layer phosphorene field-effect transistors show field effect mobility of $1000\text{cm}^2/\text{Vs}$ and an on-off ratio of 10^5 [36].

1.6.1 Bilayer Graphene

Bilayer graphene has been initially observed as a byproduct of single layer graphene exfoliation [1]. Although it is not exactly a separate material as much as the other discussed examples, the mere addition of a second graphene layer does substantially change the band structure and properties of the resulting bilayer with respect to monolayer graphene. In particular it has been observed that an insulating state can be induced bilayer graphene by applying an vertical electric field [41].

Like graphene, its bilayer has a zero band gap. However, the low-energy dispersion is quadratic rather than linear, and electrons and holes behave as massive particles unlike the massless Dirac fermions in graphene. A full review of the electric properties of bilayer graphene is given in reference [42]. Most importantly though, the band structure of bilayer graphene can be altered by means of doping or by applying a vertical electric field. This transforms the parabolic band structure into a "mexican hat" with a band gap [43, 44]. The band gap is tunable and widens as the field strength increases, saturating at a value of about 300 meV [45].

Bilayer graphene can be synthesized using similar methods as monolayer graphene, most prominently CVD[46]. The growth on copper by surface-mediated catalysis is self-limiting in principle; once a complete layer of graphene covers the substrate, precursor molecules can no longer come in contact with the Cu surface. Under the right conditions, however, before the a complete layer of graphene coalesces, a second layer can start growing underneath existing islands of graphene[46].

In the other CVD-like growth method, graphene films are formed by precipitation of carbon

[3] Phosphorene is often referred to as (monolayer) black phosphorus, after the layered bulk material from which it derives.

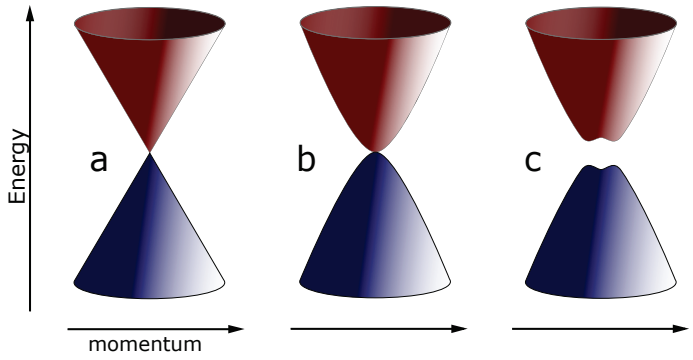


Figure 1.3 – Schematic band structure for graphene (a), bilayer graphene (b) and bilayer graphene under a vertical electric field (c). Bilayer, like monolayer graphene, is inherently gapless but when a field is applied the bands separate and create a mexican-hat-like shape. The lower (blue) parts represent the conduction bands, the upper (red) parts the valence band.

on the surface of Nickel or other metals with high C solubility. The amount of carbon that precipitates depends on a number of factors such as the C solubility, the tendency of metal carbide to form, and the cooling rate, etc. If these conditions are carefully controlled, it is possible, although challenging, to obtain exactly two layers of graphene [46].

1.6.2 Molybden Disulphide

Molybden disulphide (MoS_2) was one the first monolayer materials to be discovered in 2005, shortly after graphene, along with boron nitride (BN) and niobium diselenide ($NbSe_2$) [10]. It is also the first semiconducting monolayer material (besides $NbSe_2$) and therefore particularly interesting for electronics applications, although it was soon clear that carrier mobilities were way below those in graphene. The first report of a transistor built from MoS_2 followed in 2011 [47].

MoS_2 layers were first extracted using a similar mechanical cleavage method as was used for graphene, from bulk MoS_2, which is a layered material similar to graphite. Meanwhile, scalable production methods such as CVD growth[48, 49, 50] and liquid-phase exfoliation[51] are also available.

While bulk MoS_2 has an indirect band gap of 1.3 eV, monolayer MoS_2 has a direct band gap of 1.8 eV [52], significantly larger than Silicon (1.14 eV), which allows for high ON-OFF ratios exceeding 10^8 [47]. Mobility on the other hand was found to be relatively low $200\,cm^2/Vs$ [47]. The direct band gap makes it suitable for optoelectronic applications, for example very sensitive photodetectors [53].

MoS_2 belongs to a group of transition-metal dichalcogenides (TMDs; chalcogens are S, Se or Te), of which it is probably the most prominent representative. In a single layer TMD, the metal atoms, arranged in a honeycomb lattice, are sandwiched between two layers of chalcogenide atoms, also in a honeycomb lattice. More than 40 types are currently known, metallic and semiconducting [54]. Other notable[12, 54, 55] monolayer TMDs are WS2, WSe_2, $MoSe_2$ and

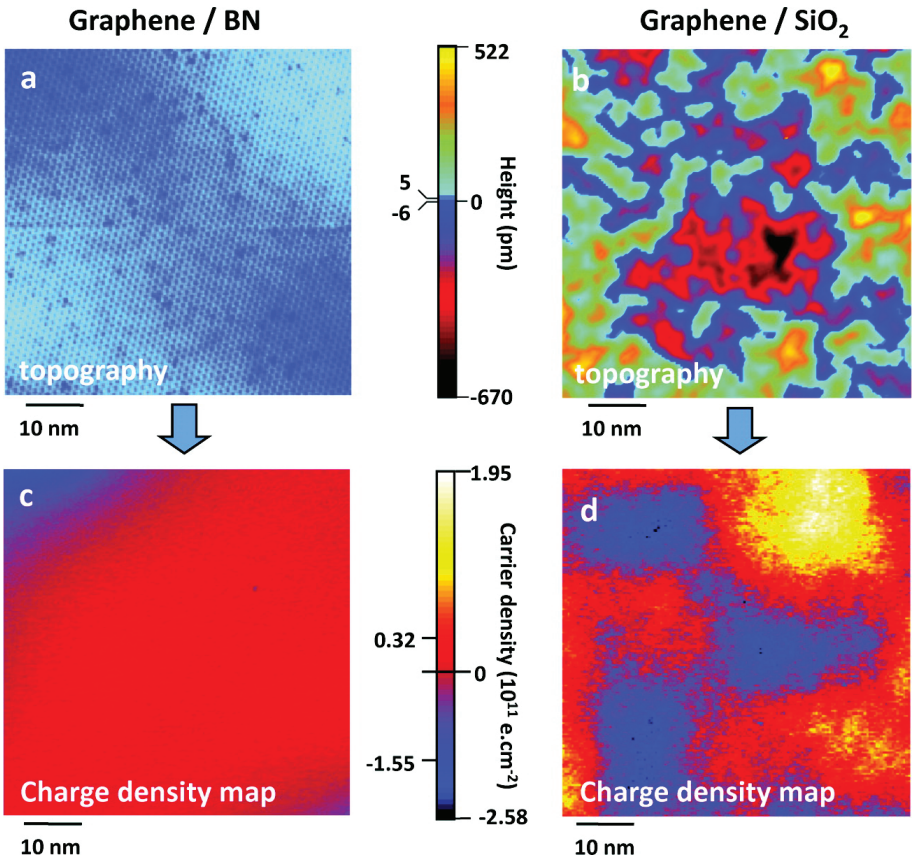


Figure 1.4 – Topography and surface charge density of graphene on h-BN and SiO_2 in comparison. Reprinted with permission from [59].

$MoTe_2$.

1.6.3 Hexagonal Boron Nitride

Boron Nitride in its hexagonal form (*h-BN*) is best known for its use as a dielectric substrate in graphene electronic devices, where it has highly favorable impact on the carrier mobilities in graphene (c.f. section 1.4.1). In fact, the use of h-BN has allowed for phenomenal transport performance to be achieved, otherwise possible only in suspended graphene samples (see table 1.1). Carrier mobilities in graphene are normally limited by impurities and phonons originating from the commonly used SiO_2 substrate [56, 57]. On hBN substrates, these effects are mitigated because hBN sheets are extremely smooth, have a crystal structure almost exactly identical to graphene and a chemically highly inert surface, with no dangling bonds or surface charges [58, 59].

BN is a III-V compound and as such very similar to carbon in many ways. The elements B and N are immediate neighbours, located left and right of C in the periodic table. Boron nitride also occurs in many of the same allotropes: The hexagonal layered structure of h-BN (with sp^2 hybridized bonds) is similar to graphite whereas the cubic form c-BN (sp^3 bonds)

corresponds to diamond and the relatively rare wurtzite form to lonsdaleite [60]. Even BN nanotubes [61] and fullerenes [62, 63] have been synthesized in the 1990's when the interest in layered materials reached its first height following the discovery of carbon nanotubes in 1991 [64].

The similarity is particularly striking between h-BN and graphene which have almost identical lattice parameters (1.44 Å in h-BN vs 1.42 Å in graphene) and interlayer spacing (3.33 Å vs 3.35 Å) [65]. There are, however, two major differences. In h-BN layers follow AA' stacking, i.e. the hexagons of two layers are exactly on top of one another (B and N atoms alternating). Graphite on the other hand has *bernal* (*AB*) stacking where every other carbon atom is centered above and below a hexagon, i.e. subsequent layers are horizontally shifted by one nearest-neighbor distance from each another [66, 67]. The other difference is that hBN has a large indirect band gap, which was very recently determined to be 5.995 eV in agreement with theoretical predictions [68], making it electrically insulating and a useful dielectric material in electron devices.

hBN can be obtained through different methods, including exfoliation [69, 70] and CVD growth, e.g. from borazane (H_3BNH_3) on copper foils [71].

1.6.4 Bandgap in 2D Materials

In the pursuit of sustaining the continued advancement of CMOS technology, the ultimate goal is to find a truly semiconducting material that allows for large on/off ratios and has high carrier mobilities enabling fast switching speed and ultimate scaling. Graphene fulfills one of the two requirements, but it lacks a band gap necessary for achieving a low off-current. This is discussed in more detail in section 1.7.1.

For these reasons, there is a strong incentive to either find a semiconducting 2D material, or to modify graphene in a way to introduce a band gap by cutting large-area graphene into nanoribbons or applying an electrical field to bilayer graphene. However, 2D materials with a band gap so far have been found to have dramatically lower carrier mobilities [47, 72, 40]. Similarly, the opening of a band gap in graphene appears to be accompanied by a systematic reduction of mobility as well [73, 74, 75, 12].

There appears to be a universal trend of mobility and band gap to be competing (figure 1.5). When a band gap is opened in graphene, the energy dispersion is no longer linear and carriers are no longer masselss [75], which implies lower mobility. It has also been observed [12], the larger the band gap of a material, the heavier the effective mass of its charge carriers. So far there has been no record of any material able to completely break out of this restriction, although Germanene may have an particularly favorable combination of a large tunable band gap [76] and high mobility [77], according to predictions.

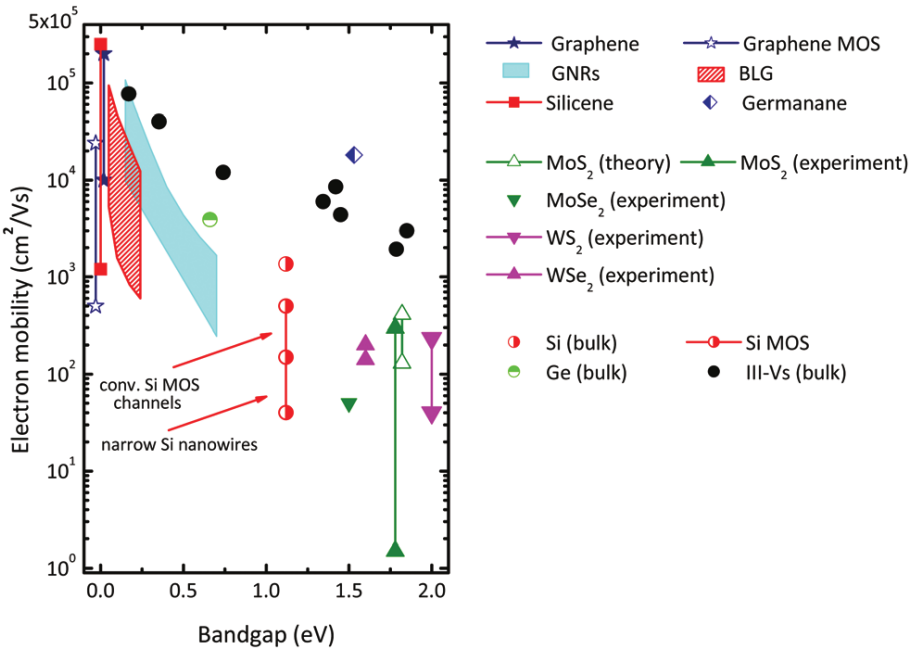


Figure 1.5 – Room temperature mobility vs bandgap for different materials, illustrating the trend of reduced mobility in materials with larger bandgaps. Graphic reprinted with permission from [12]

1.7 Applications

1.7.1 Transistors in logic circuits

According to the *International Technology Roadmap for Semiconductors*, among the key challenges to continue scaling of devices and memory, is the implementation of high-mobility channel materials in transistors. This concerns the continuation of CMOS technology, sometimes called "More Moore" strategy, for the next 1-2 decades. Currently likely candidates of such materials include Germanium for pMOS transistors and III-V compounds for nMOS transistors (typically SiGe and InGaAs) due to their high hole and electron mobilities, repsectively [78, 79, 80, 81]. Graphene far exceeds these material's performance in mobility, which remains on the order of $10^2 - 10^3 \mathrm{cm}^2/\mathrm{Vs}$.

For many years now, following device scaling into the deep sub-micron lengths, transistors have been plagued by short channel effects. In particular, *Drain Induced Barrier Lowering* (DIBL) is related to a loss of electrostatic gate control over the channel potential in very short devices, leading to leakage currents and in the worst case, preventing the device to be turned off. Strategies to improve gate control have lead to the development of ultra-thin-body SOI, FinFet and gate-all-around nanowire technologies, aiming to reduce the cross section and surface-to-volume ratio of the channel material with respect to the gate. Graphene, as a two-dimensional material would represent the ultimate surface-to-volume scaling and allow for excellent electrostatic gate control.

There are thus several aspects in favor of using graphene as a transistor channel material: its

2D geometry, the phenomenally high carrier mobility, its ability to sustain large currents and the good thermal conductivity, which is useful in evacuating waste heat. However, the inability to completely turn off current, rooted in the missing band gap, has so far been a showstopper for graphene as a serious candidate for use in logic circuit transistors.

Also crucial for proper transistor operation is the saturation of drain current for values of drain-source bias voltage V_{DS} above a certain threshold $V_{D,\text{sat}}$. This allows the transistor output to be independent of V_{DS} and to be modulated by the gate voltage alone, thus acting as a near-ideal current source. In silicon MOSFETs this phenomenon is caused by the so-called pinch off: The surface charge density in the inversion layer close to the drain vanishes leaving a highly resistive space-charge region that scales with V_{DS} leading to a constant current. This is only possible in a semiconductor with a band gap.

In order to overcome this major limitation various attempts have been made to introduce a bandgap in graphene. To be suitable for logic circuit applications, it has been estimated that a band gap of at least 360-400cm^2/Vs is required to achieve the necessary on-off contrast values [78, 82]. This can be done by lateral carrier confinement in very thin graphene nanoribbons [73, 83] or by applying a vertical electric field in bilayer graphene [44, 84]. The bandgap opening in bilayer graphene however appears to be limited (see section 1.6.1).

Larger band gaps are possible in graphene nanoribbons (GNR) but are difficult to achieve [85]: Depending on the ribbon's chirality (armchair or zig-zag edges) a width less than 10nm is required. This has been realized by "unzipping" carbon nanotubes, resulting in very precise ribbons having atomically smooth edges [73]. While this approach is ill scalable, lithographically defined structures tend to suffer from larger line edge roughness. This can lead to strong degradation of carrier transport, localized states and loss of the high mobility. An observed band gap may often be due to a Coulomb blockade resulting from the irregular ribbon edge structure rather than from the intended lateral carrier confinement [86, 87].

This loss of mobility adds on top of an inherently reduced mobility as a result of the modified band structure, which occurs independently of the technique applied to open a band gap (see section 1.6.4). Given these considerations, it appears unlikely that graphene will establish itself as viable candidate of a channel material for logic circuit transistors in a CMOS-like technology. However, beyond the more Moore horizon, graphene might still play an important role in a novel type of devices. Or might be used in different circuit topologies that leverage the high mobility without suffering from the lack of a bandgap.

1.7.2 Radio Frequency transistors

Radio Frequency (RF) and analog electronics have become pervasive in modern computers, cell phones and other electronic devices. RF transistors are building blocks in circuits such as mixers, modulators, amplifiers etc, which are essential for enabling all possible variants of wireless communication. This type of transistor has somewhat different requirements from transistors used in digital logic, making graphene a potentially suitable material.

In particular, for high frequency transistors the band-gap requirements are not as stringent

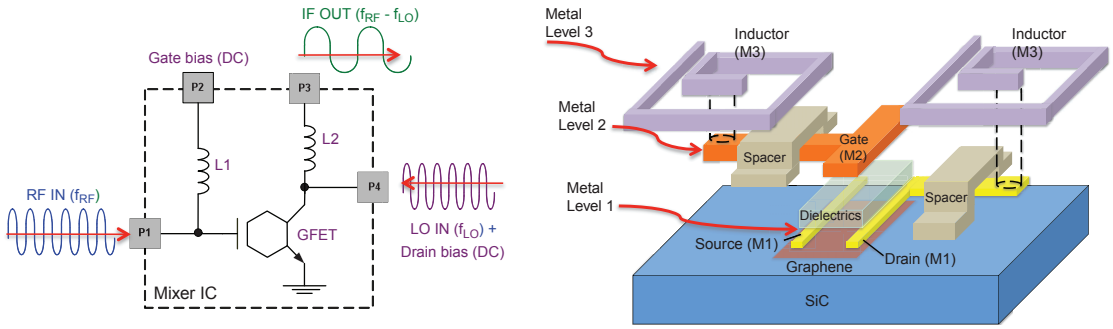


Figure 1.6 – A simple RF circuit based on a graphene field-effect transistor (GFET). Reprinted with permission from [90]

since power dissipation is a lesser concern. On the other hand, they must be capable of operating at very high frequencies. Currently the RF domain is dominated by InP, InAS and GaAs high-electron mobility transistors (HEMT), SiGe heterojunction bipolar transistors (HBT) but also Si MOSFETs [88, 89].

The inability to completely turn off current in graphene devices is not *a priori* a problem in this case, because in RF and analog circuits, the main transistor is typically biased by a constant current, defining its operating point. A small AC signal is overlaid on this DC bias and produces at the output, depending on the circuit's function, either an amplified signal or – as in figure 1.6 – a signal carrying a different frequency, which results from mixing with a second AC input.

The two principal figures of merit for RF transistors are *cutoff frequency* f_T and *maximum oscillation frequency* $f_{\max}$, where current and power gain, respectively, reduce to 0dB [78]:

$$f_T = \frac{g_m}{2\pi C_G} \tag{1.6}$$

$$f_{\max} = \frac{f_T}{2\sqrt{g_D(R_G + R_C) + 2\pi f_T R_G C_G}} \tag{1.7}$$

In equation (1.6), g_m is the transconductance and C_G is the gate capacitance. Graphene devices excel with very high cutoff frequencies[91, 92], since the carrier mobility directly factors into the value of g_m. In equation (1.7) g_D is the channel conductance, R_G and R_C are gate and contact resistances, respectively. Power gain is generally considered to be the more important figure of merit for RF circuits. Unfortunately, the values of $f_{\max}$ tend to be dramatically lower than f_T, often lagging behind by orders of magnitude [93, 23, 94].

The main reasons are the large values of g_D and the notoriously high values of contact resistance R_C, although concerning the latter, much progress has been made [95, 96]. The large channel conductance on the other hand is due to the absence of current saturation and is a consequence of the zero-bandgap, as already discussed in 1.7.1. Due to this limitation, graphene RF transistors are unlikely to be able to compete with the established technologies.

Nonetheless, the feasibility RF circuits based on graphene devices in principle has been

demonstrated in a number of cases. Examples include a voltage amplifier with a 3dB bandwidth of about 6 GHz[93], an RF mixer operating at up to 8 GHz[90], and a complete RF receiver operating at 4.3 GHz [97].

1.7.3 Flexible and Thin-Film Electronics

As discussed in the previous sections, graphene faces strong competition by traditional semiconductor materials for use in standard integrated electronics. Flexible electronics, on the other hand, are an application of growing importance where graphene has an inherent advantage over currently used materials. Bendable displays, e-paper, OLEDs and wearable electronics are examples of emerging products that could greatly benefit from Graphene's electrical and mechanical properties, in particular is large fracture strain [98].

Thin-film Transistors (TFTs) made of organic semiconductor materials are commonly used to realize circuits on flexible substrates, such as polyimide. The performance of such devices, however, is naturally very limited compared to transistors built on highly pure monocrystalline wafers. Semiconducting polymers in particular, suffer from very low field-effect mobility (less than 1 cm^2/Vs)[99]. Better performance can be achieved with polycristalline silicon or extremely thinned-down bulk semiconductors, but at the cost reduced flexibility [100, 101]. Graphene, on the other hand, is not only extremely thin and bendable but also retains a considerably large carrier mobility (several 1000 cm^2/Vs) even on these less than favorable substrates [102, 103, 104]. Nonetheless, the handicap of the missing bandgap and switch-off remains a problem, leaving flexible RF transistors as the most promising application. RF transistors with remarkably high cutoff and max. oscillation frequencies (198 GHz and 28.2 GHz, respectively) were recently reported on a flexible and transparent polyethylene naphthalate (PEN) substrate [94].

Other than for transistors, graphene can be used as a transparent electrode material in products such as touchscreens and solar panels [99]. The required properties in this case are high transparency of at least 90%, and low sheet resistance, at most 30 Ω. The primary contender in this field is indium tin oxide (ITO) which fulfills these requirements well. Graphene does have very high transparency, exceeding 97%, but achieving sufficient conductivity requires heavy doping and/or stacking of several films in parallel [30]. Its main advantage over ITO is the outstanding mechanical flexibility, chemical durability and relatively low production and deposition cost [105].

1.7.4 Other applications

Besides classical use cases in electronics, as discussed in the previous sections, graphene has been instigated for countless other applications in many domains. An overview with some select examples is fiven in figure 1.7. Relatively closely related are the fields of photonics and optoelectronics, for which graphene is suitable due to its high transparency and the extraordinarily wide and uniform spectral range of photon interaction. Graphene has been used to realize e.g. photodetectors [106, 107, 108] and optical modulators [109, 110], which

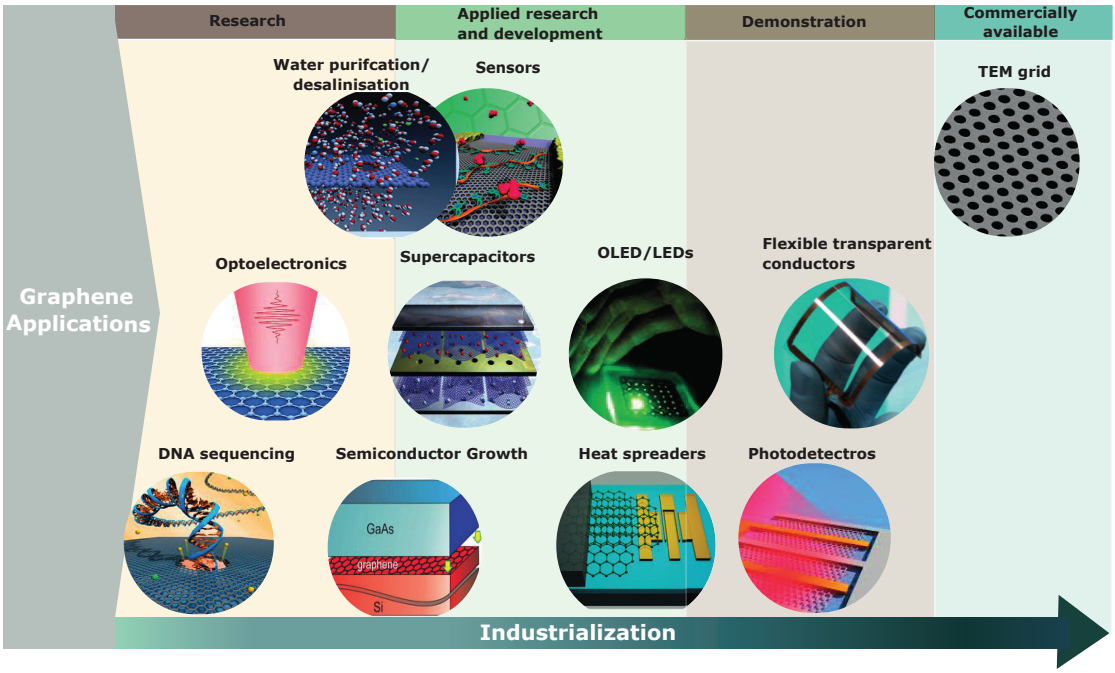


Figure 1.7 – Overview of various applications for graphene in their respective stage of industrialization. Image reprinted with kind permission by Dr. C. Moldovan from reference [115]

could be used in applications such as optical and THz-communication, optical interconnects, imaging or spectroscopy. These devices can operate at very high bandwidth because the high carrier mobility allows for particularly fast and efficient photocurrent generation [106]. Other optical devices realized with Graphene include mode-locked lasers [111, 112], polarizers [113] and very recently, a Thz non-reciprocal isolator, also known as optical diode [114], to name just a few.

Another very promising range of applications lies in the energy storage domain, where graphene, or nanocomposites of thereof, can be used as an electrode material in batteries [116, 117, 118] and supercapacitors [119, 120, 121] or hybrid devices [122]. Owing to its two-dimensional nature, graphene has an extremely high specific area (surface-to-mass ratio). Other properties that make it suitable for this application include the large intrinsic (quantum) capacitance [123], which determines the electric-double layer capacitance. Graphene also has good electrical and thermal conductivity, compared to other electrode materials, and is chemically stable, preventing corrosion in aqueous electrolytes [124]. Supercapacitors are predicted to reach energy densities on par with nickel metal hydride and lithium ion batteries, with the additional advantage of longer life-time and extremely fast charge-discharge rates [125]. Some recent realizations already achieve densities very close to these theoretical values[121, 122]. Graphene could also enhance the performance of lithium ion batteries to reach capacities double of what conventional batteries currently deliver [126].

Its mechanical properties, in particular the high Young's modulus, and large surface area per

unit mass, make graphene suitable for various NEMS[4] applications, such as switches [128] or resonators [129]. This kind of devices are typically realized by suspending single- or multilayer graphene sheets over a trench, allowing it to be electrically or mechanically actuated, enabling ultra-sensitive charge, force or mass detection [129, 130, 131, 132]. Its impermeability also makes Graphene membranes suitable for gas and pressure sensing [133, 134] capable of detecting even individual gas molecules [134]. Graphene is also hydrophobic and shows good biocompatibility, which has lead to intensive research aiming to use it for biosensing [135], in particular DNA sensors [136, 137], or drug delivery [138, 139, 140].

This short summary of applications is, of course, by no means exhaustive and the interest in graphene so tremendous that any ambition of listing every possible application would be doomed to failure. The unique collection of extraordinary properties in this material entails countless possibilities and only time will tell in which novel devices and technologies graphene will finally be utilized, but they are likely to be many.

[4] Nano-electromechanical systems [127]

2 The Graphene Field-Effect Device

This chapter covers the full range of device design, fabrication, characterization and analysis. First the techniques and tools that were used in creating the layout are presented, followed by a step-by-step explanation of the process flow and the various fabrication challenges in section 2.2. Then the electrical characterization methods are presented (section 2.3), which were used to obtain the measurement data that we analyzed by means of the empirical models given in section 2.4.

2.1 Layout

The first step, before any fabrication process can be started, is the layout design of the devices chips and wafers that are to be manufactured. The features contained in these layout designs are then patterned onto the substrate by means of lithography, which is arguably the most fundamental technique in semiconductor fabrication. The layout is designed using a dedicated computer program and stored as a collection of shapes, cells and layers in an appropriate file format. Depending on the lithographic technique and specific parameters, this data is then converted in a process called *fracturing* and translated into a format understandable by the machine that performs the lithographic writing process.

2.1.1 The Chip Layout

We designed a standard layout for the 1cm^2 square chips depicted in figure 2.1. The layout consists of an outer frame containing alignment marks and other auxiliary structures and four square regions ($3000\,\mu\text{m} \times 3000\,\mu\text{m}$) in the center. Every region contains an array of 8×9 device groups, i.e. devices with leads and landing pads for the probes used during electrical characterization.

This layout contains two types of device groups: three regions have FET-like field-effect devices consisting of a graphene ribbon, a gate and four contacts – two inner, adjacent to the gate and two outer ones – to enable Kelvin-type four terminal sensing. The third region contains special symmetric device blocks consisting of a ring-like, closed graphene ribbon with 4 gates and 4 contacts. The first device group thus has a total of 5, the latter 8 terminals.

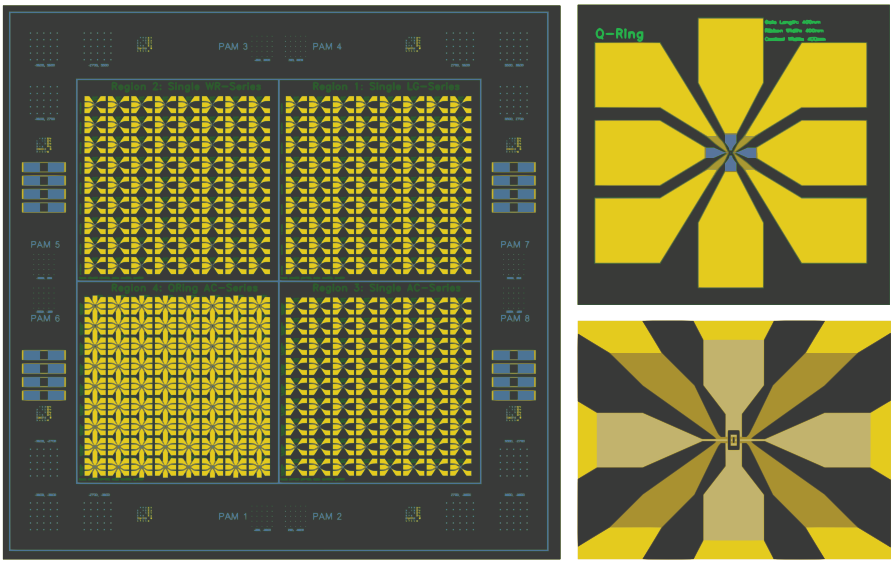


Figure 2.1 – Full graphene chip layout (left). A device group from the south-west region complete with prober needle landing pads (top-right). Zoom-in on the device core structure (bottom-right).

Parameters are varied between rows; In the NE[1] region gate lengths are varied from 50 nm to 6.4 μm while ribbon width is kept constant at 800 nm. In the NW region ribbon width is varid from 200 nm to 3.2 μm at a constant gate length of 800 nm. In the SE region devices have the same gate length but ribbon- and contact widths are varied to have a contact area increasing from 400 nm × 400 nm to 1.6 μm × 1.6 μm. Finally, the SW region, contains the 4-device blocks varying in both ribbon width and gate length (400 nm to 1.6 μm). The columns are numbered 1-8; the rows are indexed by the letters A-I.

2.1.2 Layout Software

Common layout editing tools include *Tanner L-Edit* by MENTOR GRAPHICS (which recently acquired TANNER EDA), *CleWin* by PHOENIX SOFTWARE, *LayoutEditor* by JUSPERTOR GMBH or the CASCADE *Virtuoso LayoutSuite*, to name a few. These tools offer graphical user interfaces allowing to assemble shapes by point-and-click commands, following the traditional CAD principles of EDA software.[2] They work very well for designing transistor-based circuits in rectangular shapes, using predefined layers used in standard industrial semiconductor fabrication processes. Powerful capabilities are sometimes included, such as the translation of a circuit diagram, or even the description of a circuit in a hardware definition language (e.g. *Verilog* or *VHDL*) directly into a layout. Or the verification of a layout in terms of its compliance with the design rules associated with a given technology.

The requirements for layout design in a research environment are somewhat different. Here

[1] NE: north east, SE: south east, NW: north west, SW: south west

[2] CAD: Computer Aided Design - Software packages used in various fields of engineering and architecture. EDA: Electronic Design Automation - CAD software specific to the design of electronic circuits and systems.

the design objects are individual devices or elementary circuit blocks. For the present work the needs were, in particular:

Regularity Generate arrays of devices in a regular arrangement.

Random Shapes Create random shapes, including non-rectangular.

Paremetrization Define parameters and combinations of parameters that can vary from one device to the next.

Dynamic Shapes Adapt position and size of shapes dynamically according to parameters.

Custom Layers Create and use layers ad-hoc, corresponding to the needs of a in-house specific fabrication flow.

Attributes Assign attributes to devices and other entities.

Meta Data Generate meta data, including coordinates, parameters attributes etc, that describes the layout and can be stored in a separate file.

Some of the existing tools listed above do meet one or the other requirement but it is difficult to find a tool that fulfills all of them. Advanced software suites, such as *L-Edit* or *Cascade Virtuoso* for example, provide the means to dynamically generate shapes using scripting languages, which allows for some flexibility. However, these scripting interfaces often use nonstandard languages, are limited in functionality and highly specific to the corresponding software, imposing a tedious learning curve. Lastly the mentioned software suites in this context are also very expensive.

For these reasons we opted to use *python*, a widely-used high-level, general-purpose, dynamic programming language. Python is distributed free of charge[3] and available for many operating systems. A package exists for generating, reading and writing layout data in the common GDSII layout file format. This solution allows precise and unrestricted control over the exact layout data while offering the flexibility of one of the most popular contemporary general-purpose programming languages.

2.1.3 The GDSII File Format

The GDSII (Graphics Data System II) binary format was developed in the 1970's by CALMA, a company in California, owned at the time by GENERAL ELECTRIC[141]. The format is very old and relatively primitive, but still widely in use today and sufficient for all intents and purposes in the context of this work. The GDSII format in and of itself is not particularly interesting, however it is useful to illustrate how layout data is commonly organized hierarchically in cells and layers.

A file consists of a header and a collection of *cells* and *elements*. An element can be any of seven different types:

Boundary A filled polygon: the primitive geometric element.

[3] All Python releases are open source, published under the GNU General Public License.

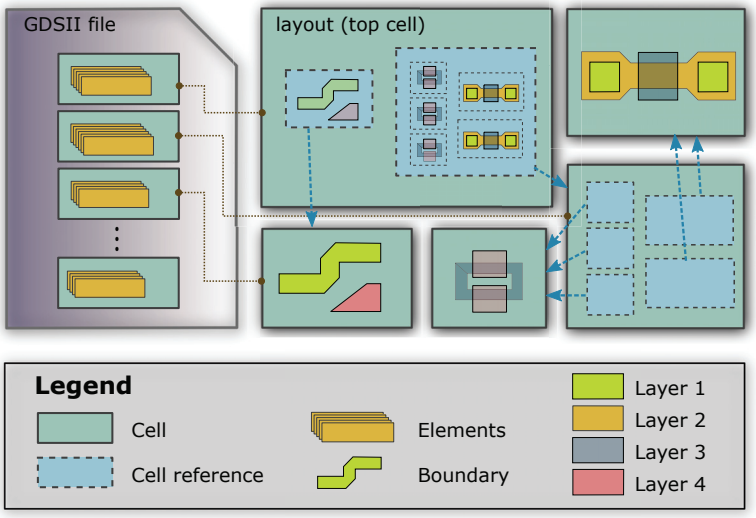


Figure 2.2 – Illustration of the GDSII format: A gds file contains a series of cell definitions. Each cell may contain a number of elements, including polygons and references to other cells. Every element belongs to a particular layer, indicated by its color. References can be nested, which allows very complex layouts to be defined from a limited number of cells definitions.

Path An open polygon.*

Cell Reference Creates an instance (copy) of a cell.

Cell Array An array of cell references.

Text A text element for documentation or labeling.*

Node Indicates an electrical net.*

Box A rectangular polygon.*

The essential element types are **boundary** and **cell reference**. The items marked with an asterisk (*) are non-writing, i.e. they are displayed on screen and can be used as annotations or to carry meta-information but will be discarded in the fracturing process. A **cell** can contain any number of other elements. Hierarchical structures are achieved by placing references to a cell inside other cells. A cell can be instantiated or copied through references an arbitrary number of times and multiple levels of nesting are possible.

A cell reference is associated with a single pair of coordinates in the enclosing structure. Cell references can be transformed through mirroring, rotation and scaling. Cell reference arrays are defined with the number of columns and rows and (optionally) with transformation parameters. All patterns to be lithographically written are represented by filled polygons defined using the **boundary** element. If text should be included in these patterns, it must be composed with boundary shapes as well; the **text** element only serves the purpose of annotation or documentation.

The GDSII format (files have the ending *.gds*) plays an important role since virtually all layout

editing programs base their operation concept on the same principles (shapes / cells / references) and the python package we use to generate .gds files also has an API very closely based on this format as well.

2.1.4 The GdsCAD Package for Python

GdsCAD is package for creating, reading and manupulating GDSII layout files. It is organized into several modules: `gdsCAD.core` defines classes representing **cell**s and the primitive elements (boundary, path, cell reference, etc). `gdsCAD.shapes` facilitates the creation of various standard shapes, such as rectangles, ellipses, polygons and writable labels using dedicated classes. The module `gdsCAD.utils` offers functions for geometric transformations and manipulating layers.

As a minimal example, is given in listing 2.1. On lines 13 and 14, a cell reference is implicitly created from `topcell` and inserted at the coordinates given by the `origin` option.

Listing 2.1 – Minimal example of gdsCAD usage.

```
1  from gdsCAD import *
2
3  # Create some things to draw:
4  text  = shapes.Label('graphene is awesome.', 200, (0, 0), layer=0)
5  box   = shapes.Box((-500, -400), (1500, 400), 10, layer=2)
6
7  # Create a Cell to hold the objects
8  fredcell = core.Cell('Fred')
9  fredcell.add([text, box])
10
11 # Create two copies of the Cell
12 topcell = core.Cell('Top')
13 topcell.add(cell, origin=(0,0));      # creates a CellReference to cell and
14 topcell.add(cell, origin=(2000,0));   # places it inside topcell
15
16 # Add the copied cell to a Layout and save
17 layout = core.Layout('testlayout')
18 layout.add(topcell)
19 layout.save('estlayout_v1.0.gds')
```

2.1.5 Python Layout Builder Framework

Besides generating the *.gds* layout file, from which the patterns for the lithography process are extracted, we also needed to produce a file containing certain meta-information, including the coordinates, parameters and attributes associated with each device on the layout. This meta-data is important for two reasons: (i) to have a map of all coordinates where a device is located in the layout (paired with information on the type of device) that is used to pilot the automated testing setup described in section 2.3; (ii) to be able to cross-reference each measurement data set with the device from which it was taken, so as to analyze the data according to the type of device and its parameters.

The entire layout is assembled from cells and cell references, as described in section 2.1.3. At the heart of the code framework is `CellBuilder` class. A *CellBuilder* instance has the

role to construct a cell from its constituent elements (geometry and/or cell references). It encapsulates the following functionality and information:

data:
- name, token and identifier
- parent `CellBuilder` instance
- subordinate `CellBuilder` instances (*"SubCells"*)
- parameters
- position: where the cell is

methods:
- `setup()`: Initialize the `CellBuilder`; define parameters and attach subcells.
- `build()`: Construct the layout **cell** from subcells and/or primitive geometry.
- `meta()`: Collect and return meta-data, including attributes and parameters.

Every `CellBuilder` class is part of a hierarchy of CellBuilders; at the top of this hierarchy is the *top cell*, which contains the complete layout. The layout is constructed by invoking `build()` on the top CellBuilder instance. This initiates a cascade from the top to bottom of the hierarchy where each CellBuilder invokes the `build()` method for each of its subcells.

The contents of a cell constructed by a CellBuilder are dependent on (i) the specific subclass[4] and (ii) the parameters provided to the CellBuilder. For every layout, region or device type a specific subclass is created. For example, assume a cell represents a region in the layout named *Region A* containing a specific arrangement of devices that are defined by a different cell *Device X*. For this purpose a class `RegionABuilder` would be derived from the base class `CellBuilder`. In `RegionABuilder` the method `setup()` would be redefined to attach a number of instances of another class `DeviceXBuilder` as subcells. Figure 2.3 illustrates this case with an added third hierarchy (everything is contained inside *Layout 0*, constructed by `Layout0Builder`).

When the method `build()` is invoked on an instance of `RegionABuilder` it will execute the default implementation provided by the base class, `CellBuilder`, which iterates over the the subcells, invoking `build()` on each instance of `DeviceXBuilder`. The method `build()` is redefined (overridden) in `DeviceXBuilder`, which does not contain any subcells but instead constructs the geometry that constitutes *device X*. In most cases, a cell builder subclass either acts as a container for subcells, defining no original geometry of its own, or it is at bottom of the layout hierarchy and constructs the actual content of the layout. A combination of both aspects is, however, possible.

Whenever a cell builder creates a subordinate cell builder, it is must supply a reference of itself to the new subcell, which stores the reference in the `parent` data member field, making it hierarchy-aware. Parameters are passed along through this hierarchy chain: A cell builder instance "inherits" (not in the OOP sense this time) all parameters from its parent. It may also define new parameters relevant to the corresponding level on which it resides. Subcells inherit

[4] Subclassing is to be understood in the sense of polymorphism in object-oriented programming (OOP).

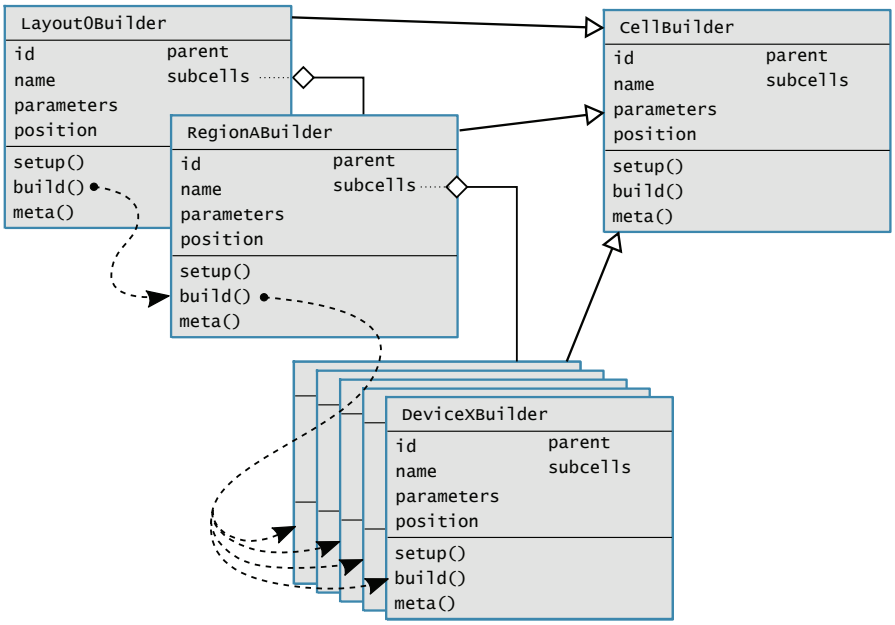


Figure 2.3 – Class diagram of the cell builder framework creating a layout with three hierarchy levels ("*Layout 0* " > "*Region A*" > "*Device X*"). The `build()` method is invoked at the top cascading through the levels until a builder class overrides `build()` or does not contain any subcells. The lines with non-filled arrowhead indicate inheritance while the lines starting with a diamond indicate aggregation (i.e. an instance of class A contains instances of class B).

these parameters as well, in addition to all those defined on the upper hierarchy levels. This concept is illustrated in figure 2.4 for the layout structure defined in section 2.1.1.

setup This method is invoked by `CellBuilder`'s constructor, i.e. it is executed only once, just after the object is instantiated. In the case of a cell that acts as a container of subcells only, this is the only method that needs to be implemented, making the class definition very simple. `setup()` is where parameters, that are relevant for the corresponding hierarchy level, are defiend and where subcells are instantiated. As soon as they are instantiated, the setup-methods of these subcells are also executed, followed by their own subcells, and so on. This causes the full set of cell builders that make up the entire layout to be instantiated recursively.

build The build method has the function of creating a **cell** object and to fill it with the elements that constitute its contents and returns it to the caller (typically the parent's build method). The contents can be **cell references** or **boundary** elements (i.e. original geometry), or both. The default implementation iterates over the subordinate cell builders (subcells), calls their `build()` methods, takes the returned cell object and places a cell reference to it into the cell being constructed, at the coordinate specified by the subcell's position data-member field. If the cell builder belongs to the lower end of the layout hierarchy, this is where the original geometry is constructed. The cell builder overrides the default implementation, creates a **cell** object and places the polygons that

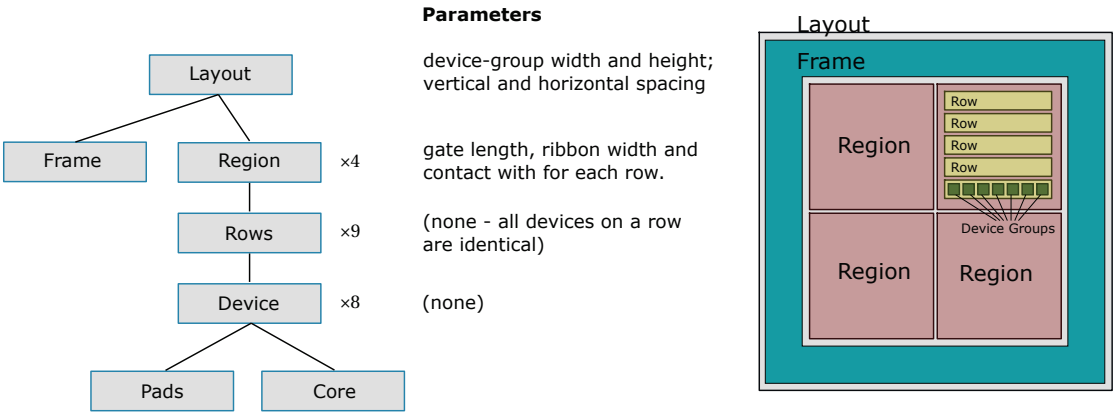


Figure 2.4 – Illustration of the hierarchy levels in our standard layout. These are realized by dedicated layout builder, region builder, row builder and device builder classes. Device size and spacing, which is uniform throughout the entire chip is defined on the layout level. Device dimensions are defined on the region level for each row separately.

make up e.g. a device structure, into that cell.

meta Like the build method, the meta method is usually implemented only at the bottom hierarchy level, and assembles a list of name-value pairs of relevant meta-data describing the entity (e.g. a device) represented by the contents created by this cell builder. Meta-data is similar to parameters, that also propagate through the layout hierarchy, with the difference that meta-data travels from the bottom to the top. The default implementation collects all the meta-data of a cell builder's subcells, concatenates it and returns the result to the calling function, typically the parent's meta method. When the `meta()` method of the topmost cell builder is invoked, meta-data from the entire layout are is collected through a cascade of meta() calls. The result is a collection of meta-data, where every device has is represented with its own data set.

Once a layout hierarchy is established and all cell builders are defined and implemented, the usage is extremely simple. To construct the layout, `build()` is called on the top-level cell builder returning the entire layout as a **cell** object, that can be written to a .gds file. A call to `meta` on the same cell builder returns the full set of meta data, which can be written to a text file.

2.2 Fabrication

Fabrication of graphene field-effect devices is challenging for various reasons. First of all, being only a single layer, the material is very sensitive to mechanical damages but also to almost any process applied, be it liquid chemicals, plasma processes or high-energy electron beam irradiation. Not to mention the procedure of synthesizing graphene with minimum defects and transferring it onto a substrate while keeping it pure and uncontaminated, which we can fortunately avoid as there are good quality commercial products available. The here presented process for a top-gated field effect device, was designed and developed with special attention to the mentioned sensitivities, while aiming at high scalability and performance. Using electron-beam lithography for high-resolution patterning allows for very small devices to be built, approaching and potentially reaching dimensions where ballistic transport becomes significant. A very thin gate dielectric grown of oxides with high relative permittivity ensures large values of transconductance, which should enable to reach voltage gains sufficient for cascading devices in a circuit.

2.2.1 Graphene Samples

Graphene is today available from numerous commercial sources and in various forms. The company *Graphene Laboratories, Inc* offers CVD grown graphene transferred onto a Silicon/SiO_2 substrate, using a well established process [31, 142, 143], resulting in a large contiguous film covering the substrate with little cracks and defects. We worked here with samples of 1 cm × 1 cm Silicon chips having a 90 nm layer of SiO_2, covered with a single layer of graphene.

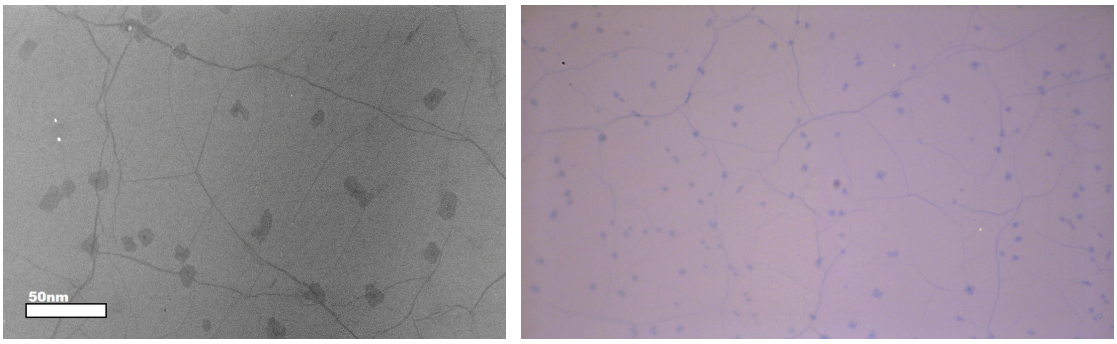


Figure 2.5 – Left: SEM image of a typical region of a sample described in section2.2.1. The darker regions are wrinkles and areas with two or more layers of graphene. Right: Optical microscope image at 100× magnification.

The graphene was grown using the method described in [31], yielding mostly monolayer graphene that also comprises wrinkles small "islands" of two or more layer-graphene (figure 2.5). These islands have a typical size (diameter) on the order of 10 µm and a spacing of several tens of micrometers. If devices with dimensions below these orders of magnitude are arranged in a regular pattern on a graphene chip, as is the case in the here-described fabrication process, the vast majority of them should be placed within an area of contiguous monolayer graphene. Although inherently undesirable, these defects are thus not a major concern, and in fact,

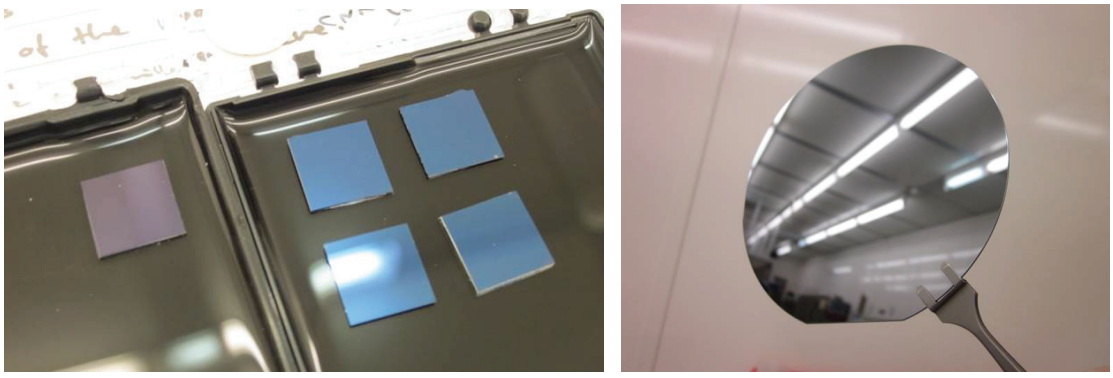


Figure 2.6 – Left: Graphene Chips in a gel-pack; Silicon substrate with a 90 nm layer of SiO_2 covered with a single layer of CVD Graphene. The four chips on the right are covered, in addition, with a Al_2O_3/HfO_2 dielectric layer, changing their color from purple to blue. Right: Bare 4-inch Silicon wafer used as carrier for the chips in many processing steps.

can be beneficial in practice, as they allow one to "see" the graphene layer in an optical or electron-beam microscope.

2.2.2 Oxide Deposition

As a first step of the process, a blanket layer of oxide is deposited on the entire chip. This layer will act as a protective layer preventing damage to the graphene layer during subsequent processing steps, and double as the insulating layer for the top gates of the field-effect devices. Since the advent HKMG technology, atomic layer deposition (ALD) has been the method of choice for growing highly uniform, conformal and defect-free high-k dielectrics for MOSFET transistor gates, both in research and industrial production.

Hafnium Dioxide HfO_2 is an excellent gate material, mainly due its high relative dielectric constant ε_r of 25 and its adequately large bandgap of 5.7 eV [144, 145]. Aluminum Oxide Al_2O_3, also long considered a viable candidate for gate dielectrics, has an even larger bandgap of 8.8 eV but a lesser ε_r of about 9 [145]. Both materials have widely been utilized in graphene and carbon nanotube electronic devices.

Because of the property of graphene of being chemically inert, direct oxide deposition via ALD on graphene has proven difficult [146, 147, 148] (although not impossible [149, 150]). A solution employed by Kim et. al. [148] consists of e-beam evaporation of a thin layer of Aluminum prior to ALD growth. This layer is then oxidized, transforming it into Al_2O_3, which acts as a nucleation layer for subsequent ALD growth.

In the process described here, we perform e-beam evaporation of a 2-3nm thick aluminum oxide nucleation layer directly from a Al_2O_3 material source, ruling out the risk of forming a non-completely oxidized Al layer on top of the graphene. After this, the samples are immediately loaded into the ALD reaction chamber where a HfO_2 layer with nominal thickness of 7nm is grown by applying 70 cycles of alternating TEMAH and H_2O precurser gas pulses. The

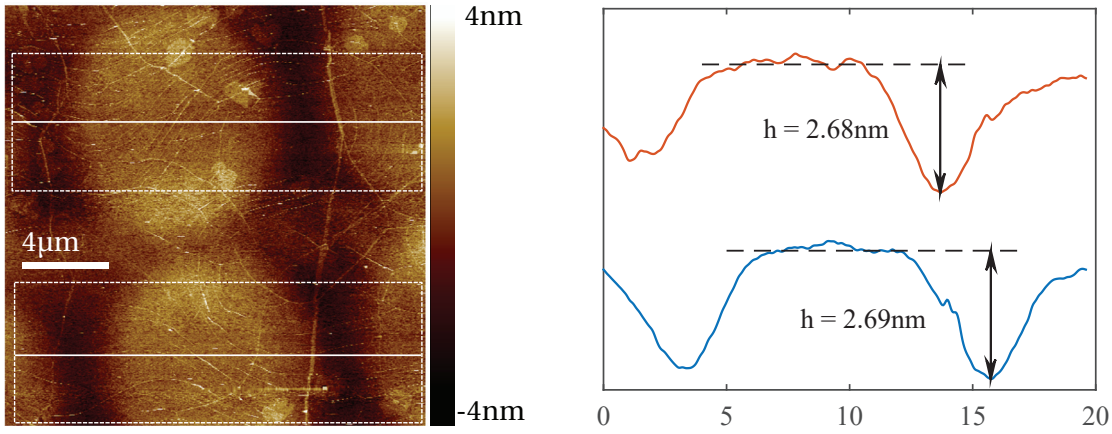


Figure 2.7 – AFM scan of Al_2O_3 evaporated through a stencil with circular openings, leading to a spot-array pattern. The deposition settings are identical to those used for the dielectric seed layer deposition, therefore the spots are expected to have the same thickness. The horizontal section profiles plotted on the right are taken from the solid lines in the afm image, averaging across the area indicated by the surrounding boxes.

resulting dielectric layer has a thickness of approximately 10 nm and thus a very thin EOT [5] on the order of 2.4 nm.

Aluminum Oxide deposition is done in a *LAB600 H* electron-beam evaporator by Leybold Optics in vacuum ($1.5\,10^{-6}$mbar) at a rate of 1 Å/s from a granular Al_2O_3 source.

Prior to depositing Al_2O_3, the substrates are in-situ heated by two ceramic radiators in the deposition chamber to a set-point temperature of 190 °C. Annealing in vacuum has been demonstrated to effectively remove resist residues on graphene [151, 152], the optimum temperature being close to 200 °C. This treatment was found to improve carrier mobility and shift the Dirac point (i.e. current minimum in the ID-VG curve of a field-effect device) close to zero[151].

2.2.3 Alignment Marks

Alignment marks are essential for any fabrication process involving multiple lithographic exposures where the different masks or patterns are to be accurately placed on top of each other. The e-beam lithography system available at *CMi* is theoretically capable of aligning patterns with an accuracy on the order of 10 nm. Practically, the accuracy depends on the quality of the alignment marks and contrast, which the EBL system is capable of extracting from a scanning electron beam image. Warping of the substrate due to other processing steps, drift from thermal contraction or expansion of the substrate, beam drift due non-optimal calibration and other effects can all induce error in the correct placement or detection of the markers, leading to misalignment.

[5] The equivalent oxide thickness (EOT) is a measure of the thickness required to obtain the same areal capacitance if the dielectric material were SiO_2 rather than the actually used high-k material. The EOT is calculated by taking the ratio of the dielectric constants $t_{eqv} = t_{\text{hi-k}} \frac{\varepsilon_{SiO_2}}{\varepsilon_{\text{hi-k}}}$

The alignment marks in this process are defined by dry etching. In order to achieve sufficient contrast for the EBL system to be able to detect the marker, a depth of about 2 µm is required. The etching process thus has to penetrate 5 layers of different materials, from top to bottom: 7 nm HfO_2, 3 nm Al_2O_3, Graphene, 90 nm SiO_2 and 1.9 µm into the Silicon substrate. There are different plasma etchers at *CMi* dedicated each to a material or set of materials.

1. The top three layers are etched in a *STS Multiplex ICP*, an inductively coupled plasma etcher from *Surface Technology Systems*, using a Cl_2-BCl_3 chemistry for 180 s.

2. Silicon Dioxide is removed in a ICP etcher from *SPTS Technologies* using a C_4F_8 plasma for 30 s.

3. The Silicon substrate is etched using in an *Alcatel AMS200* ICP system with a highly selective SF_6-C_4F_8 chemistry for 150 s.

4. The remaining resist is removed by oxygen plasama in the *STS Multiplex* for about 60 s, until the EPD signal indicates all resist has been removed.

The chemistries in these etching steps have different selectivity with respect to the electron-beam resist. The process was calibrated using optical end-point detection systems in the plasma etchers and a mechanical profiler. Steps 1-3 remove about 16, 64 and 120 nm of resist per minute, respectively, and a total of roughly 380 nm. An initial thickness of at least 500 nm of resist is thus required.

The etch mask is defined via EBL patterning of the common e-beam resist *ZEP520A*. To obtain the required thickness *ZEP* coated two consecutive times at 5000 rpm.

2.2.4 Graphene Channel Outline

The graphene evidently has to be spatially delimited to the channel and contacts region, otherwise there would be unlimited paths for current to flow around the top-gated channel region between source and drain and short-circuits between devices. Two options exist for patterning the graphene ribbons; *(i)* using a negative tone-resist and expose the regions where graphene should remain, etching everything else or *(ii)* defining the ribbon outline with a positive-tone resist such that a region surrounding the graphene ribbons is exposed and etched.

Option *(i)* has the advantage of limiting the to-be-exposed area to a minimum, leading to short EBL write times. With Hydrogen Silsesquioxane (HSQ) we also have a very good, high-resolution negative-tone resist at our disposal. However, it has been found that high energy electron beams can cause significant damage and defects to the graphene film, resulting in reduced conductivity [153, 154], making it preferable to avoid direct exposure of the channel region. In addition, the removal of HSQ after the lithography and etching process would be delicate or impossible, as the chemistry used for removing HSQ, dilute BHF, will also attack the gate dielectric materials. These arguments clearly speak in favor of option *(ii)*.

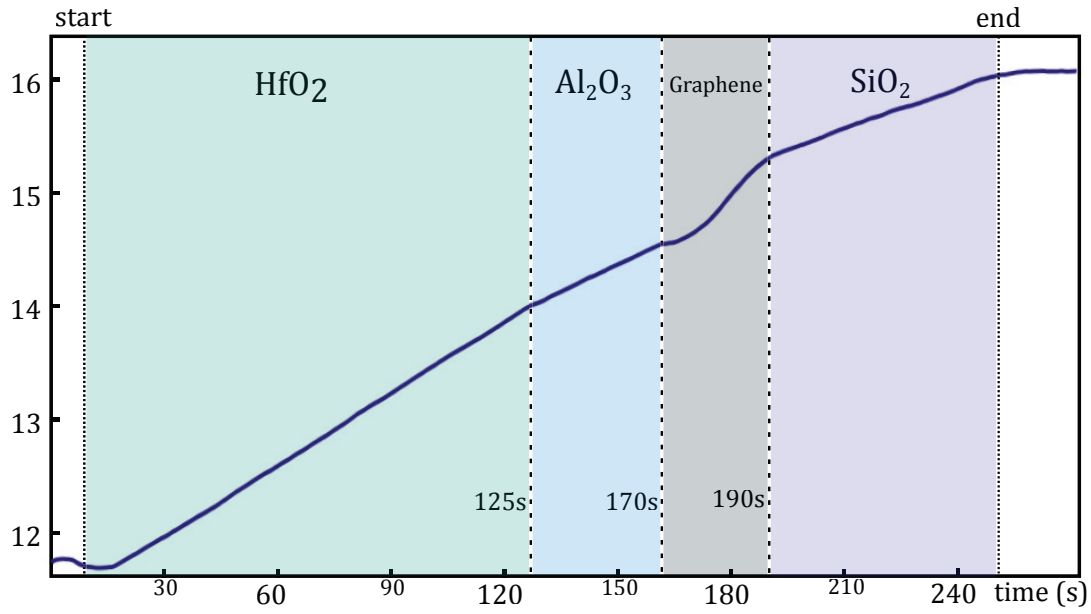


Figure 2.8 – End-Point-Detection signal recorded during a graphene outline etch in the *STS Multiplex ICP*. Four regions can be distinguished where HfO_2, Al_2O_3, Graphene and SiO_2 are being etched, respectively. The vertical axis has arbitrary units.

The etching procedure is identical to the alignment marks etching process described in section 2.2.3, except for steps number 2 and 3, which are skipped. In this process and also the alignment marks etching, the output of the end-point detection system during HfO_2, Al_2O_3 and Graphene etching (figure 2.8) is carefully monitored in order to prepare for the contacts etch described in section 2.2.5.

There is a slight kink in the EPD signal at the transition from HfO_2 to Al_2Oe etching and a steep increase as the Graphene is removed, which takes 10 to 20 seconds. Comparing the apparent etch duration for HfO_2 (~110 s) and Al_2O_3 (~45 s) with the etch rates obtained from separate measurements (see figure 2.10), we can conclude that the film thicknesses were 115 s × 4.7 nm/min = 9.0 nm for hafnium oxide and 45 s × 3.4 nm/min = 2.6 nm for aluminum oxide. This is in excellent agreement with AFM measurements (figure 2.7) and corresponds well with the intended deposition thicknesses.

2.2.5 Contacts

The source and drain contacts definition is the most delicate part of this process: An opening has to be created in the dielectric layer in all contact regions without damaging the underlying graphene sheet, so that metal subsequently deposited can form a good electrical contact. We achieve this with a combination of dry etching, wet etching and lift-off processes.

The electron-beam resist used here is a bi-layer of MMA and PMMA, designed to facilitate the lift-off process by forming an undercut in the lower layer. This undercut serves to create a discontinuity in the metal deposited on top, which allows the solvent to attack and dissolve

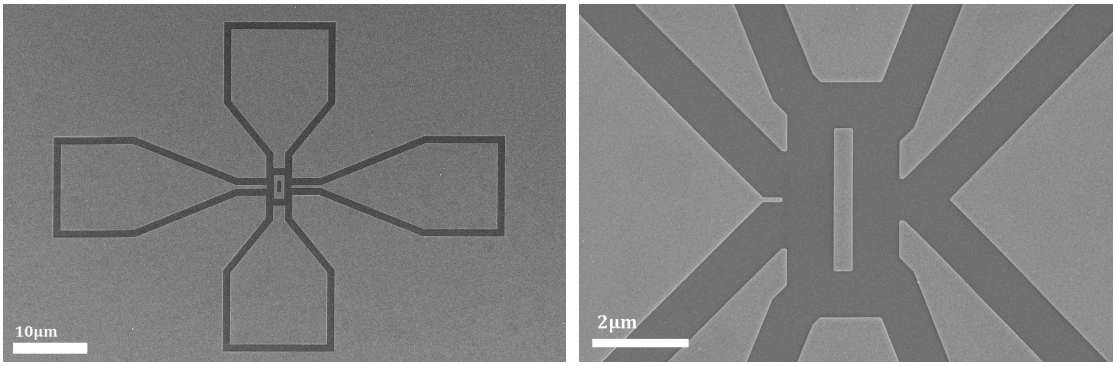


Figure 2.9 – SEM images of a four-device group with contact leads (left) and close-up of a single device region (right) after graphene outline etch. The brighter regions are where graphene and dielectric layers remain. Contact leads between device terminals and probe landing pads are also surrounded by an outline in order to prevent shorts during the contact metal definition process.

the resist beneath, allowing all metal that has landed on a non-developed region to detach and "lift off" from the substrate. By using the same resist as an etch mask and for lift-off patterning, we save one lithography step and avoid any misalignment between contact openings and metal.

The regions exposed and developed in this lithography step also comprise the intermediary leads connecting the nanometer-scale devices to the macroscopic landing pads. The actual metal-graphene contact will be formed where these regions overlap with the graphene ribbons in the device region.

The reason why a combination of dry and wet etching is necessary lies within the different etch rates of Al_2O_3 and HfO_2, and the great sensitivity of Graphene to plasma. Both oxides can be etched with dilute Hydrofluoric Acid (HF) or buffered HF (BHF), however, the etch rate of Al_2O_3 is orders of magnitude higher than HfO_2. This makes a wet etch of a stack of these materials completely uncontrollable: while it takes minutes to etch through the HfO_2, the Al_2O_3 will be dissolved in a matter of seconds. The acid will continue to attack the Al_2O_3 laterally, resulting in a disastrous delamination of the entire oxide-resist stack.

Fortunately, the relative order of etch rates is reversed in the case of dry etching: Al_2O_3 has a slightly lower rate than HfO_2. This makes it easier to remove the HfO_2 layer in the *STS Multiplex* using the same Cl_2-BCl_3 recipe as previously. The dry etch is carefully timed such that the HfO_2 layer is removed completely and the underlying Al_2O_3 layer only partially. The remaining Al_2O_3 is then removed in a very dilute BHF:H_2O solution, ensuring low etch rate and minimal or no damage to the graphene.

In order to achieve successful timing, the etch rates of Al_2O_3, HfO_2 and SiO_2 were previously assessed using ellipsometry measurements. The results of the measurements can be seen in figure 2.10. According to these experiments, the dry etch duration should be at least 90 s for 7 nm HfO_2 followed by at least 1 min of wet etching in solution (c). In practice, since there is

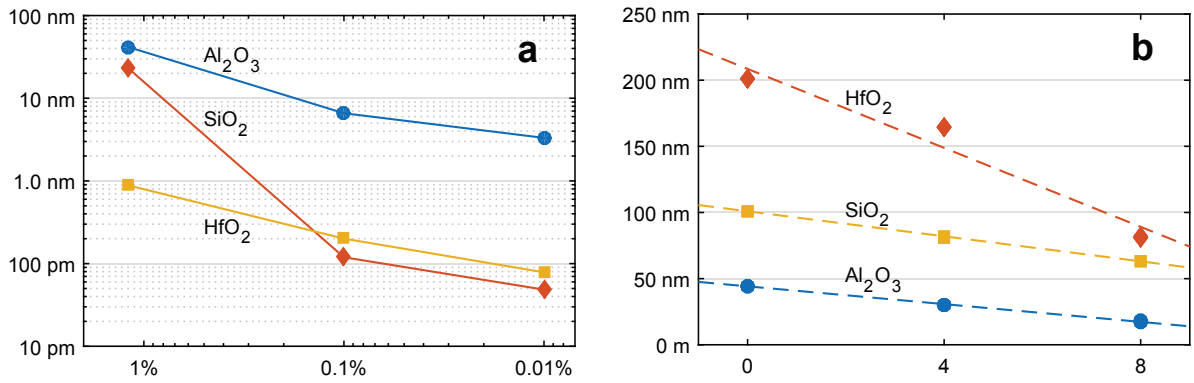


Figure 2.10 – (a) Etch rates per minute in a BHF:H_2O solution at different concentrations of HF. The etch times were 100 s in the 1.2% solution, and 10 min in the 0.1% and 0.01% solutions. (b) Measured remaining film thickness as a function of dry etch duration in a Cl_2-BCl_3-Ar plasma in the *STS Multiplex ICP* (symbols) and linear fit thereof (dashed lines).

a some uncertainty about the precise film thicknesses, these times are extended to ensure complete removal of the oxides.

Dry etch tests Baths with different concentrations of hydrofluoric acid were prepared by diluting 7:1 BHF[6] further in H_2O, such that the final, overall concentrations of HF in the solution were (a) 1.2%, (b) 0.1% and (c) 0.01%. Samples with a known oxide thickness were dipped into solutions of different concentration for a determined amount of time (solution a: 100 s, solutions b and c: 10 min). The solution chosen for the fabrication process is (c), which has a measured Al_2O_3 etch rate of about 3.3 nm/min, therefore allowing to etch the remaining Al_2O_3 in roughly one minute.

Wet etch tests Samples were etched in the *STS Multiplex ICP* for 4 and 8 minutes measuring the thickness before and after. Linear interpolation yields an etch rate of about 3.4 nm/min for the Al_2O_3 film and 4.7 nm/min for the HfO_2 film.

Following the dielectric etch, contact metal is deposited and patterned using the same MMA-PMMA mask. The material for contacts was chosen to be Aluminum, which is suitable for the lift-off process showing good adhesion, good conductivity, and is compatible with other machines in the clean-room facility following cross-contamination guidelines. With regard to the HSQ lithography step later in this process, an additional protective layer of Titanium is deposited on top of the Aluminum, which is susceptible to corrosion by the TMAH-containing HSQ developer. Both are deposited in situ in the *LAB600H* by e-beam evaporation at a thickness of 20 nm (Al) and 10 nm (Ti), followed by lift-off in an Acetone bath. The result of the process can be seen in figure 2.11.

[6] Buffered Hydrofluoric Acid (BHF) is a commonly used mixture of 49%NH_4F and 40%HF, both in water, which makes the otherwise violent etching of oxide in HF more controllable and prevents notorious resist peeling.

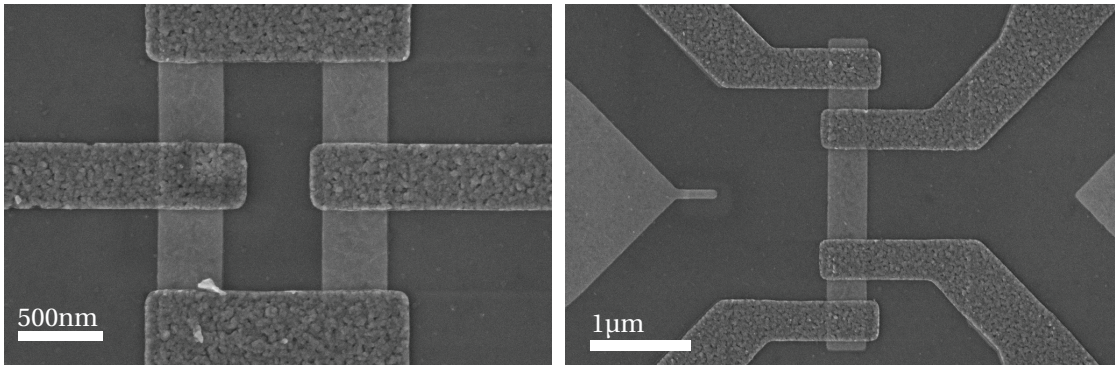


Figure 2.11 – SEM images of a four-device group with contact leads (left) and close-up of a single device region (right) after contact metal deposition and lift-off.

2.2.6 HSQ Interlayer

Hydrogen Silsesquioxane (HSQ) is an unusual, inorganic electron-beam resist. Unlike others, it consists of a network of molecules containing the elements Silicon, Oxygen and Hydrogen, rather than a carbon-based polymer. It allows for very high resolution lithography (below 10nm) and low line-edge roughness (down to 2nm) [155]. Upon exposure, HSQ crosslinks and changes into a silicon-dioxide like material, making it a negative-tone resist [156]. Unexposed HSQ can be removed with a TMAH-containing developer while removing crosslinked HSQ requires the use of HF acid. Removal is, however, not necessary, if the resist is used as interlayer dielectric material, for which it is well suited due to it's low permittivity and excellent gap-filling and planarization performance [157].

In this fabrication process, we use HSQ as an insulating layer surrounding the channel region, in order to prevent short-circuits between graphene, gate and contact electrodes. The channel is in principle covered by the gate dielectric, but the gate metal overlaps the channel laterally and could short-circuit with the graphene sheet at the channel edges. A short between contact and gate metals could form in case of pattern misalignment during lithographic write process leading the electrodes to overlap. This is increasingly likely as the spacing between gate and source/drain is reduced in the device layout design, which is desirable in order to minimize series resistance in the device caused by the ungated channel region between gate and contacts. In the presence of an interlayer this spacing could even be entirely eliminated.

2.2.7 Gate Metal

For the gate electrode definition we deposit a blanket layer of the gate metal and then pattern it by dry etching through an e-beam resist mask. Titanium Nitride (TiN) is an often used gate electrode material, can be readily etched and is, again, compatible with available equipment in the clean-room facility. TiN with a thickness of 50nm is sputter-deposited in a *Alliance-Concept DP640* magnetron sputtering system. Lithography is done by e-beam writing using a 300nm thick layer of ZEP520A. This resist being positive-tone, the gate pattern is defined by writing the outline of the gate and surrounding regions, therefore avoiding direct exposure of

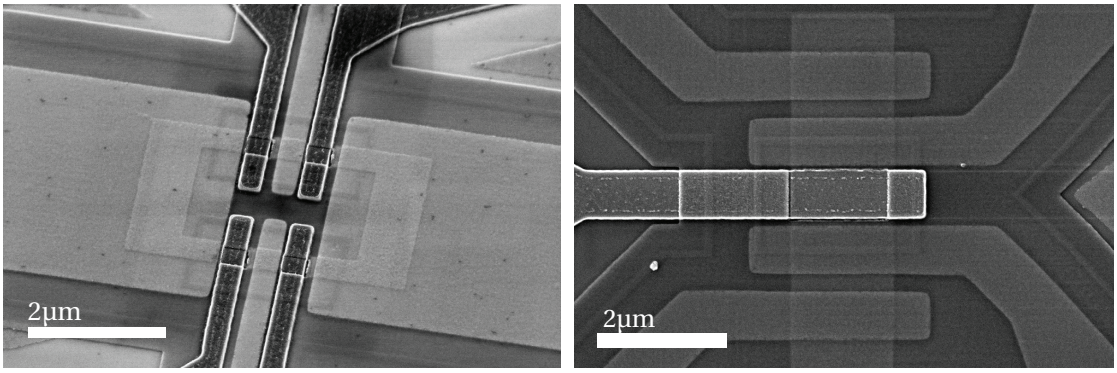


Figure 2.12 – SEM images of devices complete with contacts and gate.

the channel to detrimental electron beam radiation.

The only delicate point in this process step is to ensure that no important structures outside the gate region are damaged by over-etching the TiN layer. The etch is performed in the *STS Multiplex* by the same low-power and highly controllable Cl_2-BCl_3 process already used in the removal of dielectric layers. The optical EPD provides a clear signal as the TiN layer shows a very distinct reflection compared to the underlying materials, allowing to stop the process with adequate precision. In addition the HSQ layer previously deposited is designed to cover all regions surrounding the gate electrode and doubles as a protective layer. It thus prevents damage even in the case of a TiN overetch by several nanometers, making the entire process more robust.

2.2.8 Landing Pads

The probe landing pads are defined in a separate step, which makes it possible to use a different and much thicker material. This is important because the probe needles in the characterization setup, in order make good and stable contact, will slide across the pads when touching down. The pad material should be not too hard and have sufficient thickness. Au has been found to be a suitable material for this purpose.

The pad metal region overlaps with the contact and gate electrode leads on an area of roughly 10 µm × 10 µm at least. Before the pad metal can be deposited, it is necessary to remove the HSQ layer which still covers the contact leads in this area. We use a process similar to the contacts definition where a MMA-PMMA bilayer mask doubles as an etch mask and for patterning the metal via lift-off.

The HSQ layer is etched in buffered hydrofluoric acid, further diluted in water (BHF:H_2O 1:100), for one minute. Caution has to be exercised as the acid also attacks the Aluminum once the oxide layer is gone. We deposit a layer of 100 nm Au after a 3 nm Cr adhesion layer in the *LAB600H* evaporator, followed by lift-off in acetone. The final result of the process can be seen in 2.13.

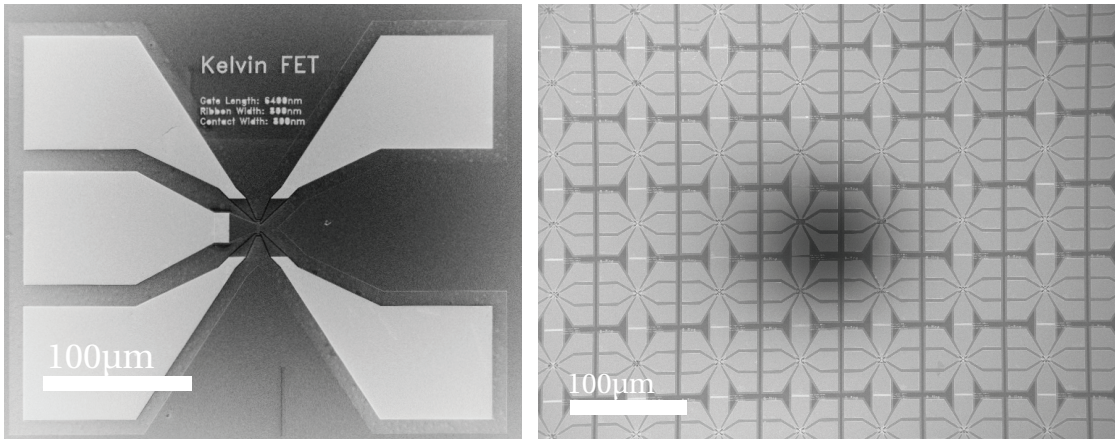


Figure 2.13 – SEM images of a complete device with five landing pads (left) and an array of four-device groups, with eight landing pads each.

2.2.9 Conclusion

In conclusion we have developed a sophisticated process that works for very thin, high-k gate dielectrics allowing the fabrication of high-transconductance graphene field-effect devices. The graphene monolayer is immediately sealed with the gate dielectric in the first process step, thus avoiding common problems of contamination with organic resist materials, which are very difficult to clean without damaging the also carbon-based Graphene. The dielectric layer also enables plasma-based processing to which unprotected graphene is very sensitive.

This approach is made possible by the carefully tuned two-step oxide etch that allows creating openings in the dielectric layer and contacting the underlying graphene without removing or damaging it. The process also systematically avoids direct exposure of the channel region during electron beam lithography which is known to induce damage that can drastically affect device performance.

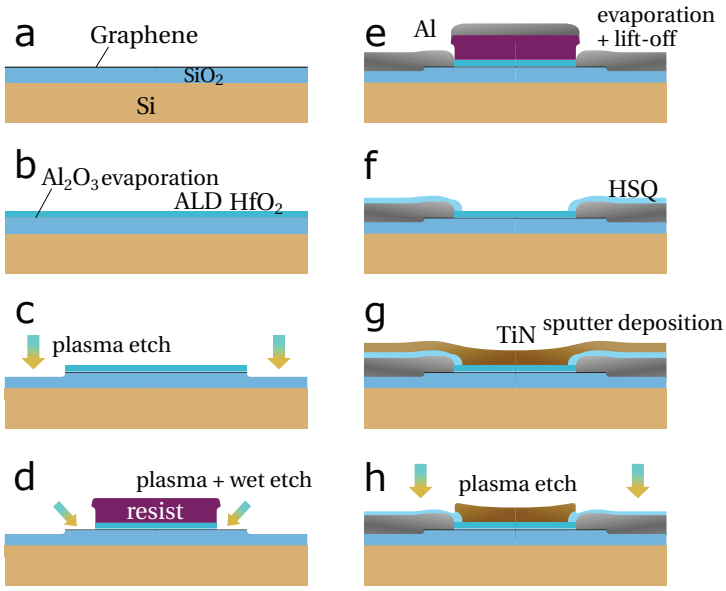


Figure 2.14 – Schematic cross-section illustration of the fabrication process.

2.3 Electrical Characterization

We have opted, in this work, for an strategy to device fabrication and testing, which optimizes the usage of the graphene sample surface, aiming at producing a maximum of devices per chip. Likewise our goal was to also achieve high efficiency and throughput in device testing by making the characterization process automated and adaptive.

There are several reasons for this approach: First, the graphene samples are quite expensive. Second, the number of fabrication process steps is independent on how many devices are built on a chip, i.e. the same effort is required for a chip having one, a few or hundreds of devices. Another reason is related to the still limited graphene sample quality due to grain boundaries, wrinkles and multi-layer islands. Having many devices ensures that through statistical probability at least a certain portion are placed in a "clean" area[7]. In addition, yield is usually limited in the case of a research/prototyping fabrication process, and some devices will always fail for various reasons, such as an accidental scratch by tweezers during handling.

Automated characterization also guarantees highly systematic, repeatable testing conditions, ensuring that all devices of a given type are subject to the exact same testing procedures. This allows to analyze data from large numbers of devices comparatively and to draw statistical conclusions. It also allows for a large amount of data to be collected form each device, which would be impossible or extremely time consuming when done manually.

2.3.1 Measurement Setup

The complete devices are electrically tested in a probe station setup depicted in figure 2.15. A Süss PA200 semi-automatic probing system equipped with a motorized chuck was used for all measurements. A series of probe manipulators are installed on the station, allowing to precisely position the needle probes on a device's landing pads, i.e. in a area of $60 \times 60\mu m^2$.

The system can be remotely controlled via the GPIB interface, allowing to change the position of the chuck. Once the needles are aligned on an initial device and the wafer's rotation is adjusted, the system can move from one device to the next in a matter of milliseconds. Since the devices are arranged on a regular, grid-like layout, going from one device to the next corresponds to a relative movement by a multiple of the inter-device distance. This makes it possible to iterate through the complete set of devices in a fully automated fashion.

The probes are connected to a semiconductor parameter analyzer (SPA, or simply *analyzer*) through triaxial cables. These instruments typically contain a set of 4 source measurement units (SMU), 2 voltage measurement units (VMU) and 2 voltage source units (VSU). The analyzer allows to operate the units synchronously and can also be remotely controlled via a GPIB interface.

The standard use is to apply a staircase voltage sweep on one of the terminals, while monitoring

[7] An alternative to this approach is to first inspect the bare graphene sample in a microscope and note down the coordinates of suitable device regions. This requires some reference structures to be created on the chip beforehand. The layout is then adapted for each chip individually placing contact and gating structures right on top of such mapped clean regions.

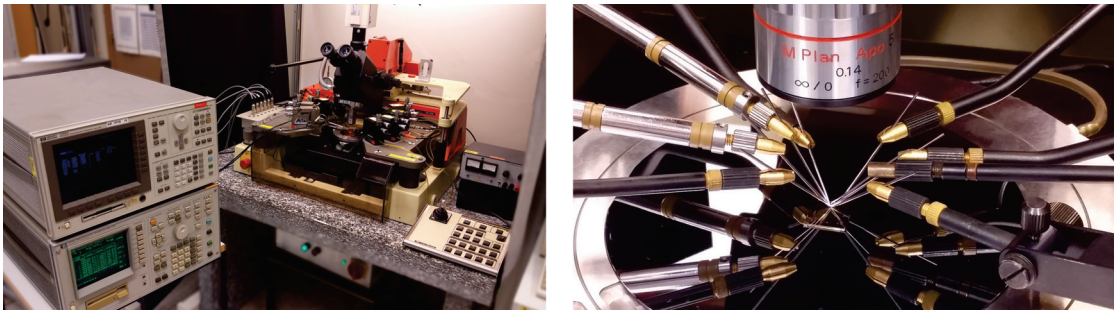


Figure 2.15 – The probe station setup; Left: Two semiconductor parameter analyzers with probe station. Right: prober needles in contact with a chip, landing on a device under test.

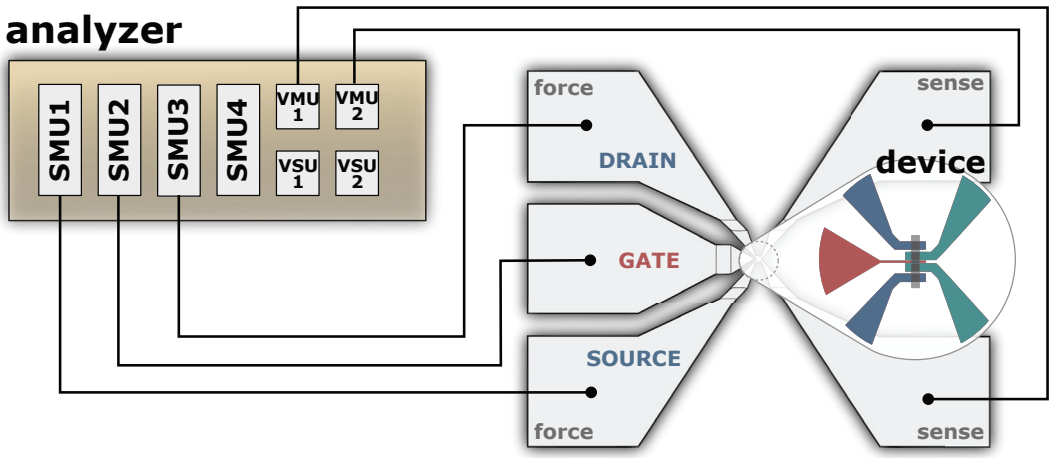


Figure 2.16 – Typical connection for DC measurements on a single field-effect device.

the others. The SMU can generate a voltage output and measure the current it is sourcing at the same time. Figure 2.16 shows a typical setup, with Kelvin-probe connections: The outer terminals are used to bias the device and measure current flowing from source to drain (*force*); the inner terminals are each connected to a VMU in the analyzer, allowing to measure the voltage between source and drain with minimal contact resistance. It is useful to have a high resolution SMU connected to the gate, measuring any possible leakage current.

2.3.2 Control Software

For this work, we developed a sophisticated electrical characterization environment based on MATLAB and its *instrument control toolbox*. MATLAB was found to be suitable for this purpose as it can be used for both testing and data analysis. Although MATLAB is not exactly a general-purpose language, it is nonetheless quite powerful, featuring relatively advanced OOP design patterns, graphical user interfaces, full control over GPIB communication, and is excellent for data visualization.

We dubbed this MATLAB program "AEC" as in *Automated Electrical Characterization*. AEC is

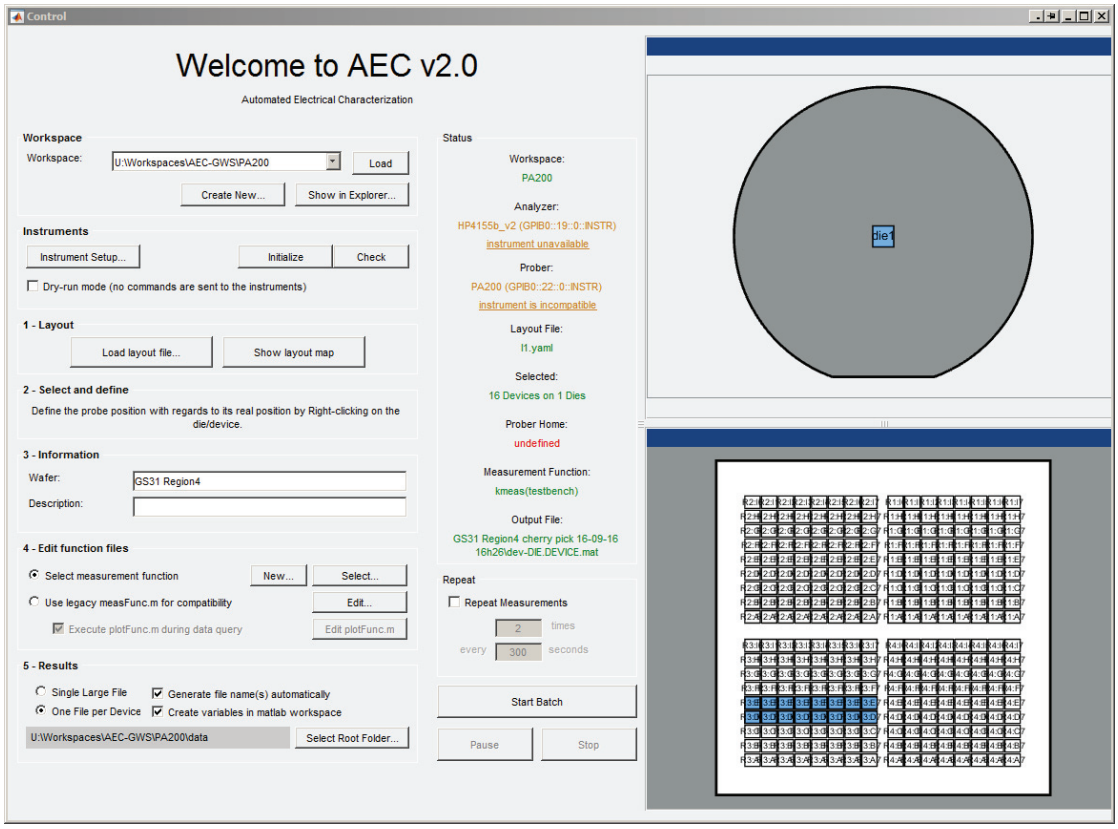


Figure 2.17 – The AEC graphical user interface.

designed to be extensible and work with different instruments and probe stations. It features a graphical user interface (GUI), shown in figure 2.17, which lets the user prepare and control a batch of customized measurements. The user interface includes a wafer-map and a die-map, visualizing the layout of the sample under test and allows to select the dies and devices to be measured.

AEC has a dual interface, consisting of an GUI on the one hand and an application programming interface (API) on the other hand. Workspace and instrument setup, layout preparation and batch execution control is done graphically, whereas the actual measurements have to be programmed in MATLAB code. This is, however, not to be considered as a drawback, but is the principal feature and purpose of the present characterization concept. Defining the measurement process programmatically allows for maximum flexibility and control, which not achievable with any other software solution.

The standard workflow when using AEC is outlined in the following:

Loading a workspace Workspaces are helpful in keeping different projects, samples types separate. A workspace is consists of a directory on the computer where settigns, instrument configurations, measurement routines and results are stored.

Instrument setup The instrument setup button opens a separate dialog where analyzer and

probe station can be selected, initialized and tested (making sure that a proper connection is established).

Layout selection Layout information is provided to AEC in the form of a layout meta-data file[8], which is generated from the *Layout Builder Framework* as described in section 2.1.5. This file contains the coordinates of dies and devices, and carrier information about each device, such as the device type and geometric parameters (gate length, ribbon width etc). This information allows AEC to draw the wafer and die maps on the right-hand side of the GUI.

Information The user may provide a sample name and a description of the measurements performed. Both will be stored together with the resulting data.

Selecting the measurement function Since measurement control is programmatic, the code to be executed is given in a matlab function file (*.m*). This file must have a specific form and accept certain parameters passed to it by AEC, such as a data set with information about the device to be measured.

Saving the results Measurement data is stored as MATLAB .mat files in the workspace directory. Options are to have one single large file containing all data, or multiple files, one for each device measured.

Status Monitor The center panel provides status information about the measurement setup. It displays whether the instruments are (i) selected (ii) reachable (iii) correctly configured and initialized. It also displays the current workspace, which layout file is loaded, how many devices are selected, the current prober position and which measurement function and output file are selected. If all items are green, the system is ready to start a measurement batch.

Batch Control Here a measurement batch can be started, paused, resumed and terminated. A repeat function allows to schedule repeating measurements with a given time interval, which is useful e.g. for endurance tests on memory devices.

Before the batch can be started, the user must, among other things, have selected a number of devices (and dies) on which measurements should be performed. From this selection, a *queue* data structure is established, containing the device objects that are to be processed. Each *device object* holds the meta-information provided by the layout file, i.e. its coordinates, device type and geometry parameters. When starting a measurement batch, a finite state machine, depicted in figure 2.18 is initiated. As long as it is in the *running* state and there is at least one item left in the device queue, the program will (i:) remove the device object from the queue, (ii:) send a command to the probe station to move to the coordinates of the current device (iii:) invoke the user-defined measurement function passing as a parameter the

[8] In the context of the electrical characterization environment, we refer to this meta-data file as the *layout file*, although strictly speaking and in the terminology of section 2.1.5, the layout-file is the .gds file containing the layout geometry.

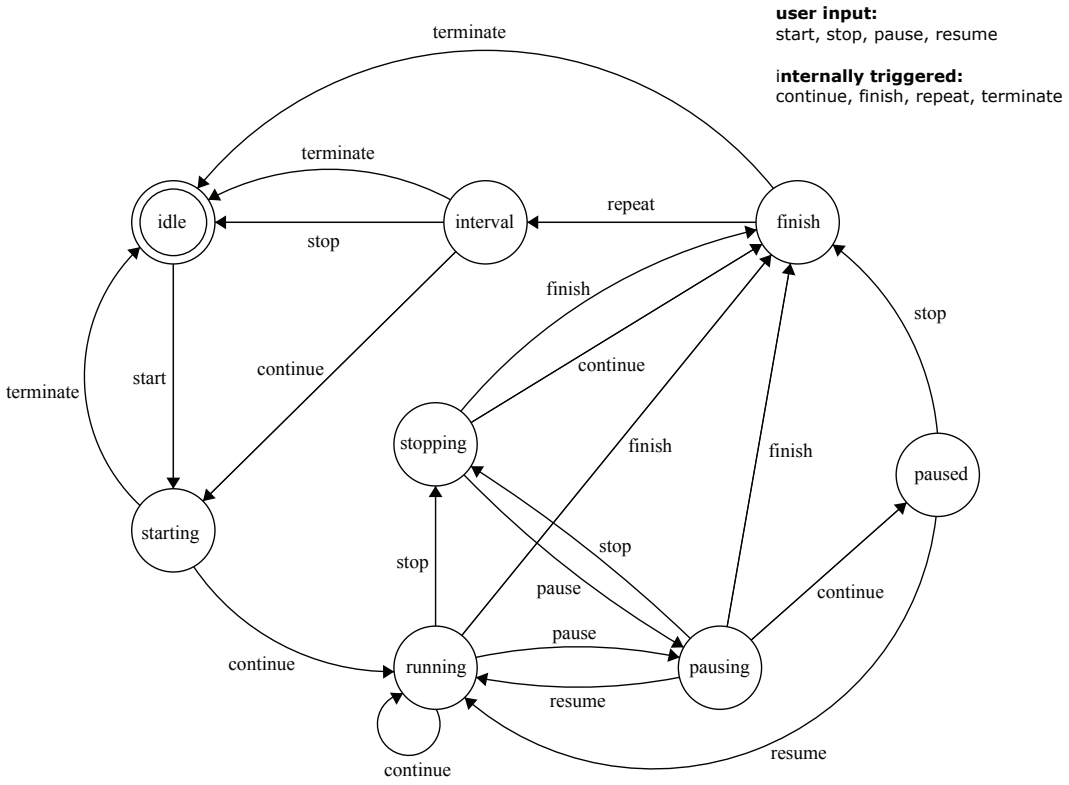


Figure 2.18 – Execution state machine for running a measurement batch.

device object then wait until measurement completes and finally (iv:) recieve a data structure containing the results from the measurement function and store in the file, paired with the device meta-data contained by the device object for future reference.

When the user-defined measurement function is executed the main argument it receives is `TestBench` object, which represents the API that AEC exposes to the user. It provides a programming interface to the measurement instruments in the form of one or more `analyzer` objects, information about the device to be measured (the *device object*), and the means to *submit* the data back to the main program with the possibility to add extra information. For example, status information can be provided, indicating whether the device testing was "successful", or if a "bad" device was encountered (short or open). As another example, if different series of sweep measurements are performed, such as IDVD and ID-VG sweeps, they can be grouped together by type.

Listing 2.2 shows a minimal example of a measurement function. In this case, the setup must be configured to work with the HP4156a semiconductor parameter analyzer. The different channels are defined as *gate*, *drain* and *source*, respectively (lines 6-9). Care must be taken that the SMUs are indeed connected to the corresponding device terminals. Once everying is set up, the measurement is started by calling the `execute()` method on the analyzer object (line 17). Adding some meta information (line 20), such as the sweep type helps identifying

the data sets later when browsing through the results in the data analysis program. On line 24, a subroutine, defined elsewhere, is called to verify, based on the measured drain current data, if the measurement has been successful or not. Finally, on line 33, the program is telling the testbench to retain the data, which concludes the measurement.

Listing 2.2 – Minimal example of a sweep measurement.

```
1   function testMeasFcn(testbench)
2       % Obtain the analyzer object
3       a = testbench.HP4156a;
4
5       % Configure the channels
6       a.resetChannels;
7       a.setupChannel('SMU1', 'gate')
8       a.setupChannel('SMU2', 'drain');
9       a.setupChannel('SMU3', 'source');
10
11      % Prepare a voltage sweep measurement
12      a.gate.setupVSweep(-2, 2, 200);  % Sweep from -2V to 2V, 200 points
13      a.drain.setupVSource(0.1);       % Drain bias: 100mV
14      a.source.setupVSource(0);        % Source: grounded
15
16      % Start the measurement
17      a.execute();
18
19      % Add some information
20      testbench.addMetaData('Measmt Type', 'ID-VG sweep');
21
22      % Verify the data and define the device status
23      I_data = testbench.getData('I_drain');
24      if checkdata(I_data)
25           % good device
26          testbench.setDeviceStatus(STATUS_SUCCESS);
27      else
28           % bad device
29          testbench.setDeviceStatus(STATUS_FAILURE);
30      end
31
32      % submit the result
33      testbench.submit();
34  end
```

Contrary to this example where only only a single sweep measurement is performed, the testing of a device can be arbitrarily complex and often involves several source files that handle different cases e.g. depending on device type. In addition, the measurement routines can be programmed such as to perform on-the-fly data analysis. For example, when measuring graphene devices, the ID-VG curve can be analyzed to determine the location of the Dirac point in terms of V_G, and adjust subsequent sweep measurements to be centered around the current minimum point at $V_G = V_0$. This is the principal strength and advantage of using MATLAB-based measurement control.

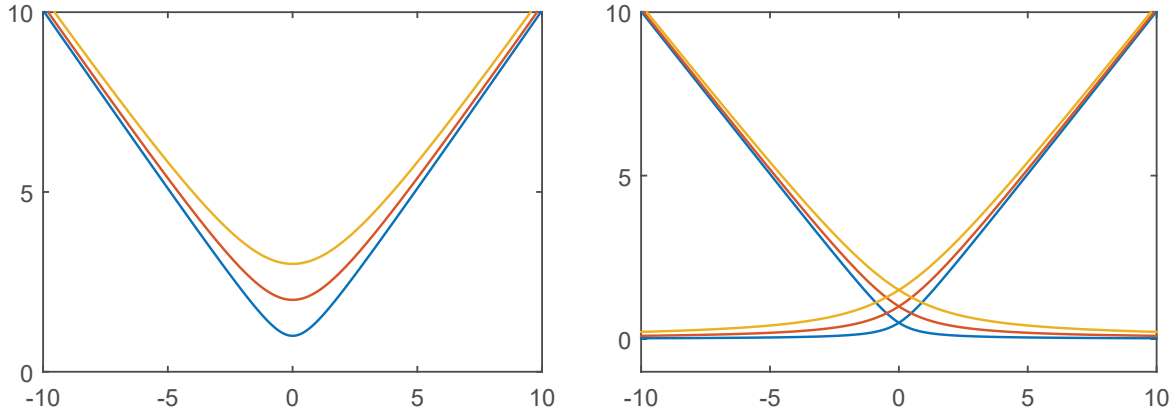


Figure 2.19 – Plot of f_V (a) and f_r (b) for different values of $\alpha = 1,2,3$. Smaller α leads to larger curvature, i.e. to a more sharp transition around the origin.

2.4 Data Analysis

2.4.1 Current-Voltage curve fitting

Empirical models commonly used to analyze measured current-voltage characteristic via curve fitting typically are designed to well mimic the 'V'-shaped appearance of a ID-VG curve, resembling what we will refer to as the (parabolic) *V-function*:

$$f_V(x) = \sqrt{1+x^2} \tag{2.1}$$

or, with parameters α and β,

$$\alpha\, f_V(\beta x/\alpha) = \sqrt{\alpha^2+\beta^2 x^2}. \tag{2.2}$$

The parameter α controls the curvature at the local minimum around the origin while β determines the slope away from $x = 0$. A similar function is the *ramp function* $f_r(x)$, which is related to the V-function through $f_V(x) = f_r(x) + f_r(-x)$:

$$f_r(x) = \frac{1}{2}\left(\pm x + \sqrt{1+x^2}\right). \tag{2.3}$$

Both functions are plotted in figure 2.19 for different values of α.

Equation (2.4) expresses the combined (electron and hole) charge carrier concentration as a V-function of gate bias, where n_0 is the residual charge concentration at zero gate voltage $V_G = 0$ and $(C_{ox}/q)V_G$ gives rise to an excess carrier concentration induced by the electric field. This model has been widely used to empirically model graphene field-effect devices, in either the here presented form or some variation thereof [158, 159, 160, 148, 16, 161, 162, 163, 164].

$$n = \sqrt{n_0^2 + \left(\frac{C_{ox}}{q} V_G\right)^2} \tag{2.4}$$

The gate voltage is referred to a reference voltage V_0 of minimum conductance which corresponds the bias point where the channel potential coincides with the Dirac point.

Dorgan et al.[161] later gave a *post hoc* justification of this approximation using definitions of the charge imbalance relation and mass-action law as follows:

$$p - n = n_{cv} = -\frac{C_{ox}}{q} V_G \tag{2.5}$$

$$pn = n_{th}^2 \frac{\mathcal{L}(\eta)\mathcal{L}(-\eta)}{\mathcal{L}(0)^2}. \tag{2.6}$$

Equation (2.5) defines the field-induced (n_{cv}) and (2.6) the thermal (n_{th}) carrier concentration. $\mathcal{L}$ is the solution of the Fermi-Dirac integral for graphene and η the normalized Fermi energy. The authors then replace the right-hand side of (2.6) with a constant n_0 representing the minimum carrier density resulting from an averaging of thermal carriers and spacial charge "puddles". Combining (2.5) and (2.6) results in a quadratic equation which yields

$$n, p = \frac{1}{2}\left(\pm n_{cv} + \sqrt{4n_0 + n_{cv}^2}\right). \tag{2.7}$$

This variant of the *V-function* model allows to account for electrons and holes separately, turning it into a *ramp function*, and is used in [148, 161, 162].

Some authors use (2.4) or (2.7) as an integrand in evaluating the current [159, 163], whereas in other cases [148, 164] it us used to directly model the channel conductance by multiplying with $q\mu$, the elementary charge and carrier mobility and a scale factor W/L according to the device's geometry. By assuming the channel conductance to be proportional to carrier concentration [165, 24], the total conductance of the device can be written as $R_{dev} = 2R_c + R_{ch}$, the sum of contact resistance and channel resistance, where R_{ch} has the form of

$$1/R_{ch} = \frac{W}{L} q\mu \sqrt{n_0^2 + n_{ex}(V_G)}. \tag{2.8}$$

Here, n_{ex} is the excess carrier concentration as a function of V_G. This excess carrier concentration is generally the linear relation found in (2.4) but can also be more complex, as in [148] where a square-root term $\hbar|v_F|\sqrt{\pi n}/q$ is added, originating from quantum capacitance [10, 166] as explained in [167].

The model used in this work is essentially the same, with the distinction of using a different notation, which lends more emphasis to the fact that parameters reflect apparent effective phenomena rather than physical properties and is geared towards usage in circuit design and analysis:

$$G_{ds} = \sqrt{g_0^2 + g_m'^2 (V_{gs} - V_0)^2}. \tag{2.9}$$

Here, $G_{ds} = 1/R_{ch}$, g_0 is the minimum or "base" conductance at the Dirac point ($V_{gs} = V_0$) and g_m' is the "reduced" transconductance, i.e. the transconductance per unit of gate voltage $g_m' = g_m/V_{gs}$. We use lower-case indices (gs, ds) to indicate intrinsic quantities that relate

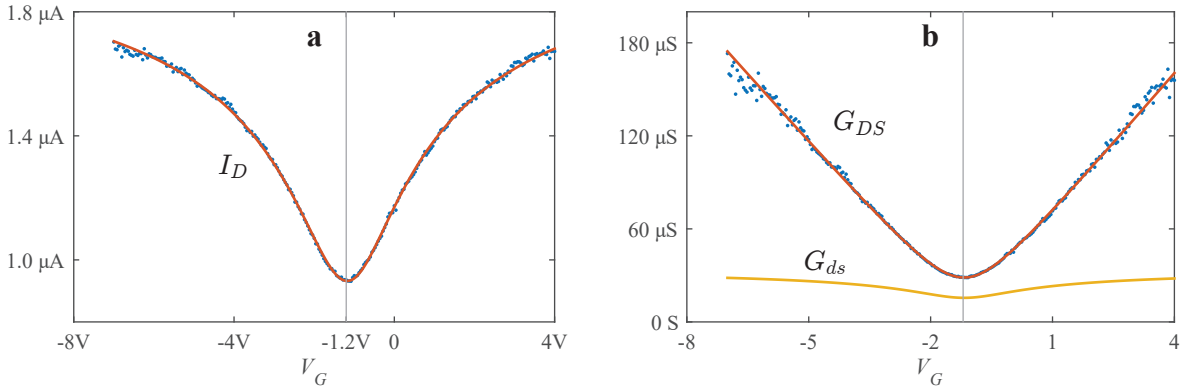


Figure 2.20 – Current-Voltage plot of an V_G sweep measured on a top-gated graphene field effect device, biased at $V_D = 60\,\text{mV}$ (a). Intrinsic channel conductance (upper curve) and extrinsic device conductance, including contact resistances (lower curve) (b). The solid line in (a) is a fit obtained with (2.12), the dots are measured data. The intrinsic conductance is obtained from equation (2.11). The Dirac point is located at $V_G = -1.2\,\text{V}$ and the series resistance is $R_s = 2R_c = 29\,\text{k}\Omega$.

only to channel conductance modulation, and upper case indices (GS, DS) where the contact resistances are taken into account. The total device conductance is

$$G_{DS} = \frac{G_{ds}}{1 + 2R_c G_{ds}} \tag{2.10}$$

or, conversely

$$G_{ds} = \frac{G_{GS}}{1 - 2R_c G_{DS}}, \tag{2.11}$$

and the drain current

$$I_{DS} = G_{DS} V_{DS} = \frac{G_{ds}}{1 + 2R_c G_{ds}} V_{DS} \tag{2.12}$$

which is the most basic fitting expression for ID-VG curves with parameters g_0, g'_m, R_c and V_0. An example of measured current-voltage data analyzed using this model is given in figure 2.20. Using the relation (2.11), the intrinsic conductance can be de-embedded and one retrieves the predominantly linear dependence of conductivity on gate voltage (and carrier concentration) that has been observed since earliest studies [1, 10] and has been studied in some detail e.g. by Hwang et al.[165] and Chen et al.[24]. Conversely, the typical sublinear bending and eventual saturation of current (figure 2.20a) in ID-VG measurements can be attributed to the effect of contact resistance.

Combining equations (2.4), (2.8) and (2.9) one can extract the field effect mobility from the

fitting parameter g'_m, which is consistent with the commonly used expression [82]:

$$\mu = \frac{L}{W}\frac{g'_m}{C_{ox}} \tag{2.13}$$

In summary, the V-function model covers the most important phenomenological aspects of a graphene field effect device yielding excellent fitting results and provides a reliable way of extracting the field-effect mobility and series resistance from measured data. The other two parameters g_0 and V_0 contain useful information on residual charge density, doping and fixed charges.

Major limitations of the V-function model include the rigid symmetry with respect to V_0, which does not allow, for example, to consider different values of mobility for electrons and holes. On the other hand, the model exhibits an unphysical asymmetry with respect to the device terminals, as only the gate-source voltage is taken into account in the expression of the field effect, leaving out the gate-drain voltage completely. It also ignores the fact that the minimum conductance point varies as a function of drain and source potential $V_0 = V_0(V_S, V_D)$.

2.4.2 Advanced empirical modeling

2.4.2.1 Conductance asymmetry

Real devices often show an asymmetry where the electron and hole branch of the ID-VG curve have different slopes, i.e. different values of g'_m, as shown in figure 2.21. This phenomenon has received some attention [168, 169, 170, 171, 172] and is most likely due to Fermi level pinning in the graphene under the contacts. Depending on the metal workfunction, the graphene in the contact regions is set to be of n or p type, independently of the gate bias. If for example this pinning leads to n-type contact regions and the gate bias induces a p-type channel, then the device will be in a $n-p-n$ configuration with two highly resistive $p-n$ junctions. In the case of an n channel however, the devices will be in a $n-n-n$ configuration without any junctions leading to much higher overall conductivity.

While a more phenomenologically accurate description may be warranted, it can be convenient to simply attribute the asymmetry to different transconductances and/or (apparent) mobilities of the two carrier types. In the case of such asymmetry, our model based on the V-function obviously falls short and a simple remedy is to split the model into two cases and, for simplicity, define $g_n = g'_{m,n}$ and $g_p = g'_{m,p}$, the transconductances for electrons and holes, respectively. Given that (2.9) can be written as $g_0 f_V(g'_m v)$ where $v = (V_{gs} - V_0)/g_0$, we can analogously write:

$$G_{ds} = \begin{cases} g_0 f_V(g_n v) & V_{gs} > V_0 \\ g_0 f_V(g_p v) & V_{gs} < V_0. \end{cases} \tag{2.14}$$

While this approach is sufficient for simple fitting problems, it introduces a discontinuity at $V_G = V_0$ that can cause convergence problems if the model is to be used for circuit simulations.

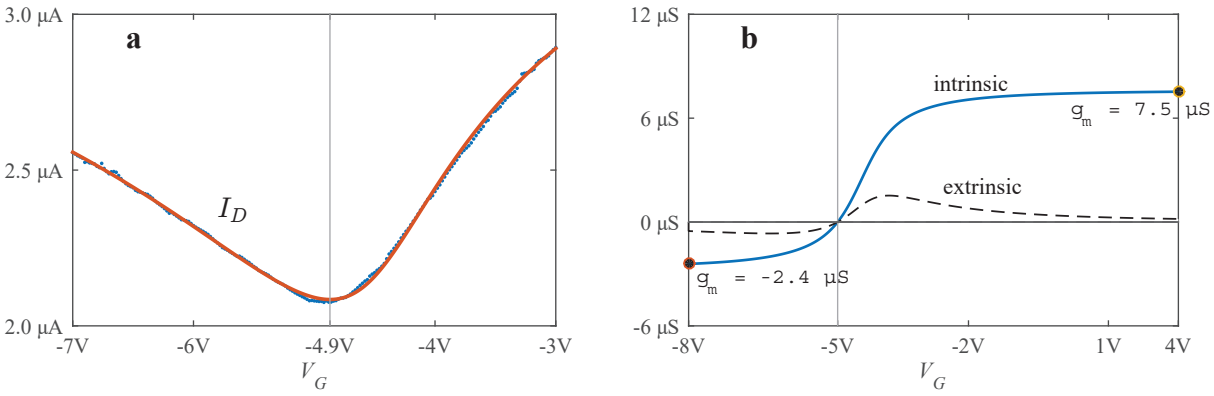


Figure 2.21 – Asymmetric ID-VG characteristic of a measured graphene field effect device. The electron branch shows roughly three times higher conductivity than the hole branch (dots are measured data, solid line is a fit obtained with (2.15)) (a). Intrinsic transconductance extracted using the same fitting model (solid line) and extrinsic transconductance, as obtained by deriving $\partial G_{DS}/\partial V_G$ (dashed line) (b). The device was biased at $V_D = 100\,\mathrm{mV}$.

A more elegant solution is to replace the V-function with a ramp function, defining G_{ds} as

$$G_{ds} = g_0 f_r(g_n v) + g_0 f_r(-g_p v). \tag{2.15}$$

This model is continuous and infinitely differentiable over all values of v and allows for accurate fitting, as shown in figure 2.21.

2.4.2.2 Improved current model

Habibpour et al. [163] proposed a semi-empirical model based on the V-function, computing the drift current by integrating from source to drain:

$$I_{ds} = q\frac{W}{L}\int_{V_{gd}}^{V_{gs}} \mu_{\text{eff}} n(V)\, dV. \tag{2.16}$$

In this case, the variable V is defined as the local, position-dependent voltage in the channel $V = V_G - V_{ch}(x) - V_0$ while $n(V)$, the combined electron and hole concentration, is otherwise defined as in (2.4). Further, μ_{eff} is a field-dependent effective mobility, saturating when the local electric field $\vec{E}$ exceeds a critical value. The field, however, is approximated as $|\vec{E}| = V_{ds}/L$ to be independent of the integration variable and taken out of the integral.

The integral of $f_V(x)$ is

$$F_V(x) = x\sqrt{1+x^2} + \log\left(x + \sqrt{1+x^2}\right) \tag{2.17}$$

and thus the solution to (2.16) is

$$I_{ds} = I_0\left(F_V(v_{gs}) - F_V(v_{gd})\right) \tag{2.18}$$

where $v_{gs} = \frac{C_{ox}}{qn_0}(V_{gs} - V_0)$, $v_{gd} = \frac{C_{ox}}{qn_0}(V_{gd} - V_0)$ and $I_0 = qn_0\mu_{\text{eff}}\frac{W}{L}\frac{qn_0}{C_{ox}}$. This approach is more physically solid than assuming a lumped channel conductance directly proportional to n. In particular it reflects the symmetry of the device between source and drain, which now can both have arbitrary voltages.

In order to account for different electron/hole mobilities, the author of [163] divides the domain of the current-voltage characteristic into four quadrants, where V_{gs} and V_{gd} are either smaller or larger than V_0. In each quadrant, I_{ds} is computed as in (2.18), replacing μ_{eff} with an electron or hole-specific effective mobility, according to the corresponding majority carrier type. The different terms are then connected together using tanh-based analytic step functions in order to avoid convergence problems in simulations.

An alternative to this approach is, again, to use a ramp function instead of the V-function, the integral of which is:

$$F_r(x) = \frac{1}{2}\left(x f_r(x) + \log(f_r(x)) + 1\right). \tag{2.19}$$

Electron and hole current can now be separated:

$$\begin{aligned} I_{ds} = &\quad I_n + I_p \\ = &\quad I_{n_0}\left(F_r(v_{gs}) - F_r(v_{gd})\right) \\ &+ I_{p_0}\left(F_r(-v_{gs}) - F_r(-v_{gd})\right) \end{aligned} \tag{2.20}$$

This results in largely the same quantitative I-V characteristic but in a more compact form and without the need for step-function stitching together the separate terms. The resulting ID-VG curves can be seen on figure 2.22. Compared to the simple conductance-based model (2.15) this approach treats the graphene channel as a continuum with a local channel potential varying between source and drain.

It is interesting to note that the base function F_r has a dominant term $\propto x^2$, leading to a $\propto V_G^2$-like behavior in the majority branch ($V_G > V_0$ for electrons, $V_G < V_0$ for holes). However, when all the relevant terms are put together, the electron current, for example, is approximately $\propto (V_G - V_S)^2 - (V_G - V_D)^2$ causing the V_G^2 terms to cancel such that the linear-like dependency on gate voltage is retrieved in the ID-VG characteristic. This is the reason why both carrier concentration and current in graphene devices show the same, roughly linear behavior.

It should also be noted that the second term in (2.20), $\log(f_r(x))$, is negligible with respect to the first. Moreover, it is likely more physical to omit this term as it leads to negative values of electron (hole) current for $V_G < V_0$, ($V_G > V_0$). The integration constant 1/2 is chosen to ensure that $\lim_{x\to-\infty}\frac{1}{2}\left(x f_r(x) + 1\right) = 0$.

2.4.2.3 Surface I-V fitting

Using the improved empirical model described in the previous section, it is possible to analyze of the complete current-voltage characteristic including all terminals of the graphene field-

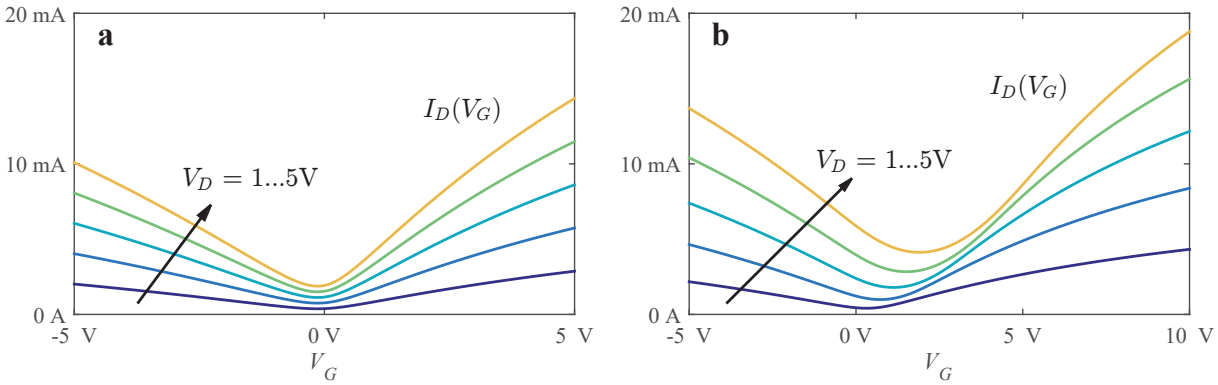


Figure 2.22 – Comparison of ramp-function conductance model (2.15) (a) with the modified Habibpour's function model (2.20) (b) with asymmetric electron and hole transconductances ($g_n = 800\,\mu$S/V, $g_p = 500\,\mu$S/V, $g_0 = 400\,\mu$S, $R_S = 100\,\Omega$, $V_0 = 0$). Both plots show a set of ID-VG curves with V_D increasing from 1V to 5V in steps of 1V. The model in (b) correctly predicts the Dirac point shift as a function of V_{DS} and the broadening of the current valley bottom between V_S and V_D.

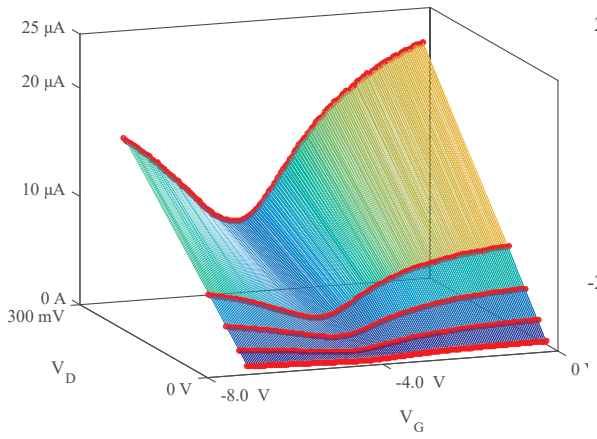
Dirac Point:	$V_0 = -4.2$V
Series Resistance:	$R_S = 10\,$kΩ
Transconductance:	
electrons:	$g'_{m,n} = 42\,\mu$S/V
holes:	$g'_{m,p} = -18\,\mu$S/V
Base conductance:	
electrons:	$g_{0,n} = 45\,\mu$S
holes:	$g_{0,p} = 19\,\mu$S

Table 2.1 – Fitting parameters obtained from the data shown in figure 2.23a.

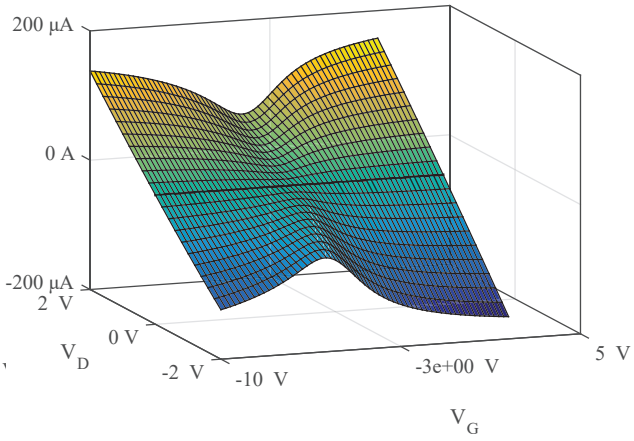
effect device. The underlying measurement data is a series of ID-VG voltage sweeps, obtained by applying a different, constant drain voltage for each sweep that is step-wise incremented, while keeping the source voltage grounded. These are complemented by a series of ID-VD sweeps, where gate voltage is incremented between sweeps, and source again is kept at zero bias. A surface fit is obtained by concatenating these measurements and applying the fitting algorithm to obtain a single set of parameters for the entire series of sweeps.

The results of this fitting process applied to a device are presented in figure 2.23. The model applied in this case was the modified Habibpour's empirical model (2.20). The fitting parameters obtained for this device are listed in table 2.1. It is noteworthy that transonductance and base conductance have similar values and we will see later that there is a correlation between these parameters.

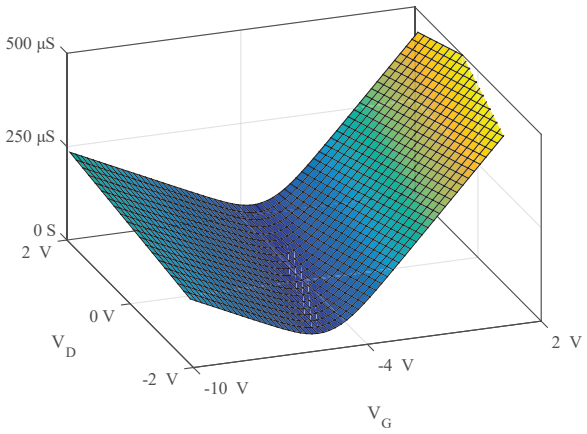
It can also clearly be seen in the figures, in particular 2.23c, that there the valley representing the conductance minimum is tiled with respect to the V_D axis. For low values (or large negative



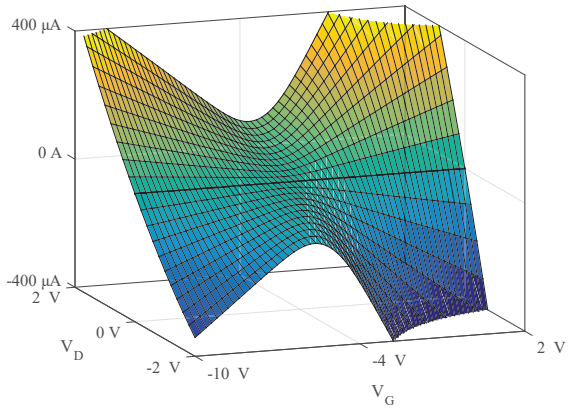
(a) Surface-plot of a series of ID-VG sweep measurements. The red dots are individual measurement points. The drain voltages are 10 mV, 30 mV, 60 mV, 100 mV and 300 mV.



(b) Current-Voltage characteristic extrapolated from the ID-VG sweep measurement surface fit of the data shown in figure 2.23a. The thick black line marks the $V_D = 0$ bias condition, resulting in zero drain current.



(c) Surface-plot of a the intrinsic drain-source conductance G_{ds} obtained and extrapolated from the data in 2.23a.



(d) Current-Voltage characteristic extrapolated from ID-VG sweep measurement surface fit. This surface plot shows the I-V characteristic that would result if the same device had much lower access resistances $R_S = 100\,\Omega$.

Figure 2.23 – Sweep measurement data and current/conductance surface plots obtained from the same fit based on the said data.

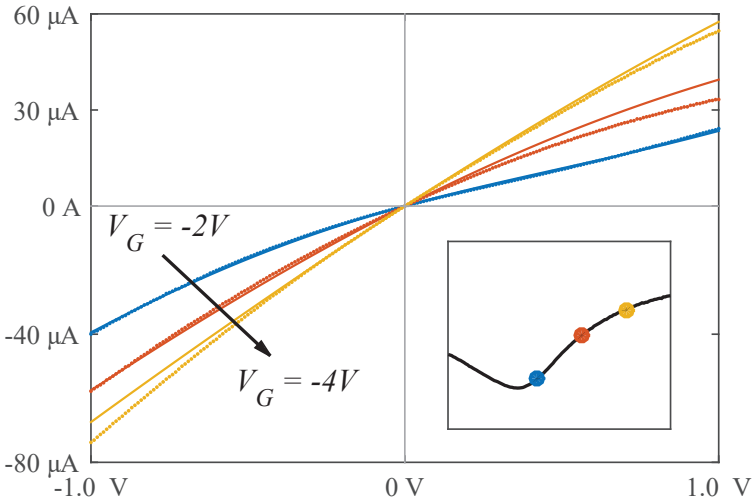


Figure 2.24 – Drain current vs drain voltage (ID-VD) curves. The dotted lines are data obtained directly from ID-VD sweep measurements. The solid lines are ID-VD curves computed from the ID-VG surface fit in figure 2.23. The gate voltage bias values are −4 V, −3 V and −2 V and are visualized as circular markers on the reference ID-VG curve in the inset; the marker of $V_G = -4$ V being the one closest to the Dirac point.

values) of V_D the minimum occurs at a slightly lower value of V_G and for large values of V_D the minimum occurs at a slightly larger value ov V_G. This dependence of the Dirac point on drain bias has already been seen in figure 2.22b and is directly responsible for the commonly observed 'kink' in the ID-VD characteristic of graphene field-effect devices, which is discussed e.g. by Meric in [159].

The kink effect can also be seen in our ID-VD measurements, although it is mitigated by the relatively large contact resistance of our devices and the limited range of drain voltage sweeps between ±1 V. Figure 2.24 shows a series of as-measured ID-VD curves together with ID-VD curves computed from the ID-VG surface fit shown in figure 2.23. The accuracy is somewhat decreases for larger values of V_D which is related to the fact that the ID-VG fit is based on data where the range V_D is limited to values $\leq 0.3V$. Nonetheless, the agreement between curves, particularly in the range between ±0.3 V and where V_G is close to the Dirac point, is fairly good and can be regarded as a validation of the used model.

2.4.3 Conclusion

We have seen an overview of techniques for analyzing measurement results obtained from standard DC sweep measurements, namely ID-VG and ID-VD sweeps. The most primitive approach, given by using a V-function, has proven to be a good basis for more elaborate functions, which are obtained by taking into account series resistance and electron-hole

branch asymmetry. It has also been, to some extent, physically justified by means of simplified relations for charge imbalance and a mass-action law. In its most advanced form, which is obtained from integrating over channel length, the model can successfully describe the full, three-terminal I-V characteristic of the graphene device, resulting in a surface fit which is in agreement with both, ID-VG and ID-VD curves simultaneously. Following these results, the model was also found to be useful for describing behavior of graphene devices in a small circuit as described in the following chapter.

3 A Graphene Circuit Study

3.1 The differential Circuit

Graphene "transistors", as has been explained in the introduction, suffer the drawback that no complete turn-off can be induced. Even in a perfect device at bias conditions, which should lead to minimal (theoretically zero) carrier concentration at the Dirac point, there is a considerable minimum current. According to the observations made in section 2.4 the current minimum also increases with larger drain-source bias.

Since the efficiency of modern CMOS circuits relies heavily on he high on-off ratios in silicon MOSFET transistors, it is clear that without a bandgap, the graphene transistor is unsuitable as an element for CMOS-like circuit topologies. We propose here a building block that could be used to realize the full set of Boolean functions without relying on the conventional turn-on/turn-off paradigm.

The circuit block consists of a strip of graphene forming a base branch (stem) that is split into two upper branches. The current in each of the upper branches is controlled by a gate fabricated on top, and connected to a load resistor. The gated regions of the upper branches each form a current-modulating graphene field-effect device, while a constant-current source connected to the stem controls the base current. Depending on the input signals at the gate on either branch, the base current is directed into one or the other branch where the load resistors produce a differential output voltage. Figure 3.1a illustrates this concept using familiar circuit element symbols, where the transistor designates a graphene field effect device.

The circuit thus operates on a differential input signal (fed into the gate electrods) and produces an differential output signal, which only relies on the *ratio* of currents between the two branches - a complete turn-off is not needed. This same principle has been successfully utilized in very high-speed bipolar ECL (emitter-coupled logic) and MOSFET SCL (source-coupled logic). It is also ubiquitous in analog circuit design, known as the differential pair.

3.2 Device Model for Hand Calculation

In order to qualitatively understand the behavior of the proposed differential circuit we use the following empirical model, that was already discussed in the previous chapter. Reasonable

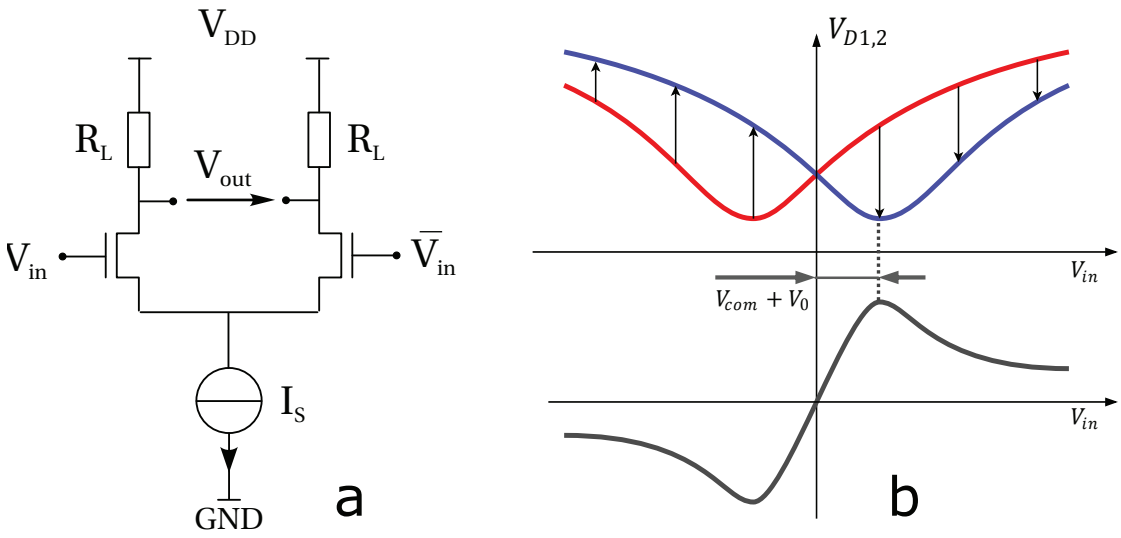


Figure 3.1 – Circuit schematic (a) and simplified working principle of the graphene differential block (b). Upper axis: left (red) and right (blue) transistor output (drain) voltage, V_D. Lower axis: Transfer curve, V_{out}, determined by subtraction of blue curve from red curve.

values for the parameters are later selected according the results of analysis performed on the measurement data from fabricated field-effect devices using an essentially identical model for curve fitting:

$$G_{ds} = \sqrt{g_m'^2 (V_G - V_0) + g_0^2} \tag{3.1}$$

where G_{ds} is the transistor's overall conductance between source and drain, g'_m is the transconductance per unit of drain-source bias ($g'_m = g_m / V_{ds}$), V_0 is the Dirac voltage, and g_0 is the conductance minimum at the Dirac point ($G_{ds}(V_G = V_0) = g_0$). For simplicity g'_m and g_0 will be referred to as reduced transconductance and base conductance respectively. This intrinsic conductance translates into an extrinsic output current, when taking the contact resistances into account ($R_S = 2R_C$).

$$I_{extr} = V_{DS} G_{ds} (1 + R_S G_{ds}) \tag{3.2}$$

These are responsible for the concave bending and eventual saturation of the $I_D(V_D)$ curve far away from the Dirac point. No other current saturation effects, such as carrier velocity saturation due to scattering mechanisms (MOSFET-like pinch off does not exist in gapless single layer Graphene[173]), are taken into account here.

This simple model, albeit empirical rather than based on physics principles, provides excellent fitting results and allows extracting parameters that reflect the device's extrinsic performance

relevant for circuit simulation. Similar models, also containing square-root based expressions but tailored to extract physical rather than circuit-relevant parameters were used in the past, e.g. by Meric [159, 16] and Scott [162]. It may also be more suitable for hand calculations in the analysis of elementary circuits than complex physical models. Combining a series of $I_D(V_G)$ curves, measured at different drain bias values, and performing a surface fit allows capturing the complete DC characteristic of a device. Surface fits obtained in this manner exhibit a slightly larger residual error compared to individual curve fit but are still acceptable for our purpose (Figure 3).

3.3 Differential circuit analytical modeling

The working principle of the differential circuit block relies on a constant current source in the stem and two switching devices directing the current in either one or the other of two "branches" (Figure 4). The sum of the currents of both branches is therefore constant. The switching effect can be described by an imbalance factor α.

$$\alpha = \frac{I_1 - I_2}{I_S} \tag{3.3}$$

where $I_S = I_1 + I_2$ is the stem current supplied by the constant current source. In this formulation, the branch currents become

$$I_{1,2} = \frac{1}{2}(1 \pm \alpha) I_S \tag{3.4}$$

The output voltage is the difference of the drain nodes in either branch of the circuit.

$$V_{D1,2} = V_{DD} - R_L I_{L1,2} \tag{3.5}$$

$$\begin{aligned} V_{out} &= V_{D1} - V_{D2} \\ &= R_L(I_2 - I_1) \\ &= -\alpha R_L I_S \end{aligned} \tag{3.6}$$

If we model the graphene devices as conductances G_1 and G_2 (which are each a function of the devices' bias conditions, i.e. V_G) then the total resistance of each branch can be expressed as

$$R_{br,i} = R_L + 1/G_i \tag{3.7}$$

Since the voltage drop on both branches is necessarily identical, we can write $R_{br1} I_1 = R_{br2} I_2$.

Combining this with equations (3.4) and (3.7) yields

$$\frac{R_L + 1/G_2}{R_L + 1/G_1} = \frac{1+\alpha}{1-\alpha} \tag{3.8}$$

which can be rearranged and solved to find the imbalance factor, as follows

$$\alpha = \frac{G_1 - G_2}{G_1 + G_1 G_2 R_L + G_2}. \tag{3.9}$$

This result is independent of the bias conditions V_{DD} and I_S and reflects the circuit's intrinsic performance. For G_1 and G_2 we can substitute a modified version of equation (3.1) in which we replace $V_G = V_{com} \pm V_{in}$ respectively, where V_{com} is the common offset voltage around which the input voltage V_{in} is varied. Note that, as a simplification, the (common) source voltage, V_S, is not taken into account. Whereas the relevant parameter for the channel conductance modulation is $V_{GS} = V_G - V_S$ rather than simply V_G we assume here a source voltage of 0V in order to maintain the analytic expressions at a manageable complexity. In practice, for numerical computations, we select a value of V_{com} to which we add the term $V_{DD} - I_S(R_L/g_0)$ thus compensating for a nonzero, constant V_S. The circuit's transfer function is

$$V_{out} = H(V_{in}) = -\alpha(V_{in}) R_L I_S \tag{3.10}$$

The transfer curve is schematically illustrated in figure 3.1b. Its appearance is dominated by the subtraction of the output characteristic of one device with the other's, resulting in a useful, linear region between a negative and a positive peak value. These peaks correspond to the Dirac point of each device respectively, their position on the input voltage's axis is related to $V_{com} + V_0$ as illustrated in the figure. The principal figures of merit of this differential block are the input swing, characterized by the relative distance between the Dirac peaks in the transfer curve, as well as the slope and linearity of the linear region in-between. The slope can be computed by taking the derivative

$$S'(V_{in}) = \frac{\partial}{\partial V_{in}} R_L \alpha(V_{in}) \tag{3.11}$$

Note that S' is the slope per unit of bias current, I_S, bearing the unit $1/A$; we define the actual slope as $S = I_S S'$. The result is rather unwieldy but can be evaluated at $V_{in} = 0$, resulting in

$$S'(0) = \frac{g_m^2 R_L}{G_0^2 + R_L G_0^3}(V_0 - V_{com}), \tag{3.12}$$

where $G_0 = \sqrt{g_m'^2 (V_0 - V_{com})^2 + g_0^2}$.

Parameters that can be independently tuned to optimize the circuits' performance include the common mode of the input signal V_{com} and the pull up resistances R_L. Figure 3.2 displays the slope versus each of these parameters. In order to maximize the slope, there is an opti-

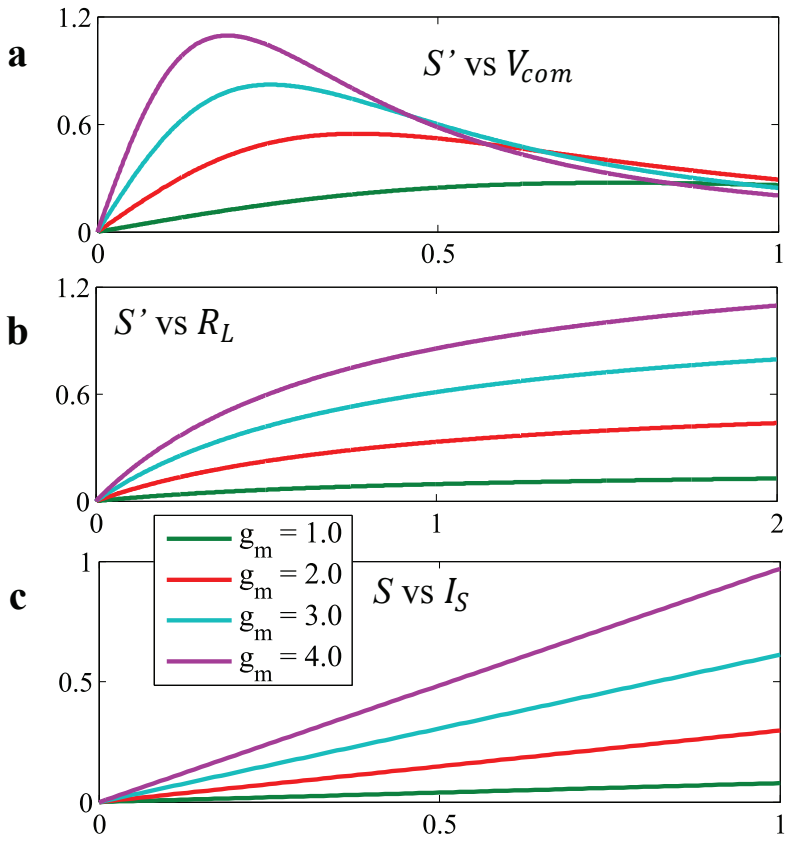


Figure 3.2 – Slope S' of the transfer curve at $V_{in} = 0$ for different values of g_m, as a function of (a) V_{com} and (b) R_L and (c) S as a function of I_S. Variables are normalized according to table 3.1.

Parameter	Unit	Typical Value		Normalization Factor		Normalized Value
g'_m	S/V	800	µS/V	400	µS/V	2
g_0	S	400	µS	400	µS	1
V	V	1	V	1	V	1
I_S	A	400	µA	400	µA	1
R_L	Ω	2.5	kΩ	1 / 400	µS	1
S'	1/A	2.5	μA^{-1}	1 / 400	µA	1

Table 3.1 – Typical values and normalization of main parameters. All parameters of a particular unit share the same normalization factor.

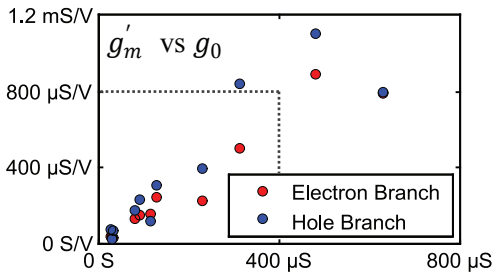


Figure 3.3 – Scatter plot of the reduced transconductance g'_m vs the base conductance g_0 of a multitude of devices with varying dimensions.

mum value for V_{com} beyond which not only the slope but also the linearity decrease. This optimum value can be very close to the symmetry point ($V_{in} = 0$) and approaches it further as transconductance improves. In terms of the load resistance, the slope monotinically increases with the value of R_L, but the benefit of incresing R_L further diminshes gradually as the slope approaches its asymptotic value.

Theoretically, both R_L and I_S could be multiplied at will in order to boost the circuit's amplification. However, the value of V_{DD} required to keep the current source from saturating may quicly reach prohibitive levels. Instead it will be advisable to carefully tune the balance between R_L and I_S such as to obtain an effective drive current while limiting the voltage drop across the load resistors.

For realistic numerical modeling, it is crucial to assess the relationship between the model's two main parameters, g'_m and g_0. Measurement data presented in Figure 3.3 reveals a linear trend where $g'_m \approx \chi g_0$, with the proportionality constant $\chi = 2$. This trend is interesting since it is desirable to have both a high value of g'_m and a low value of base conductance, g_0. It appears, however, that it is not possible to improve one of the parameters independently of the other. The values in Table 1 are chosen accordingly.

3.4 Circuit simulation results

With the same model and the coefficients obtained from a surface fit of a series of ID(VG) as well as ID(VD) curves, we programmed a compact model in Verilog-AMS for use with a circuit simulator, in this case CADENCE/Spectre. This approach allows for more flexibility as well as complexity in the circuit design compared to the analytical derivations. In particular it allows taking the contact resistances into account that tend to be on the order of the base conductance.

The results depicted in figure 3.4a show a fairly linear transfer curve in the input voltage range roughly between -1V and +1V, depending on the bias current. The tradeoff is between input swing and voltage gain (steepness of the transfer curve), which reaches a slightly amplifying value of 1.4. Here we adjusted I_S and R_L for a supply voltage level of 5V.

In order to achieve higher values of the amplification factor, we analyzed characteristics of graphene FETs previously reported. We found that devices with very low values of g_0

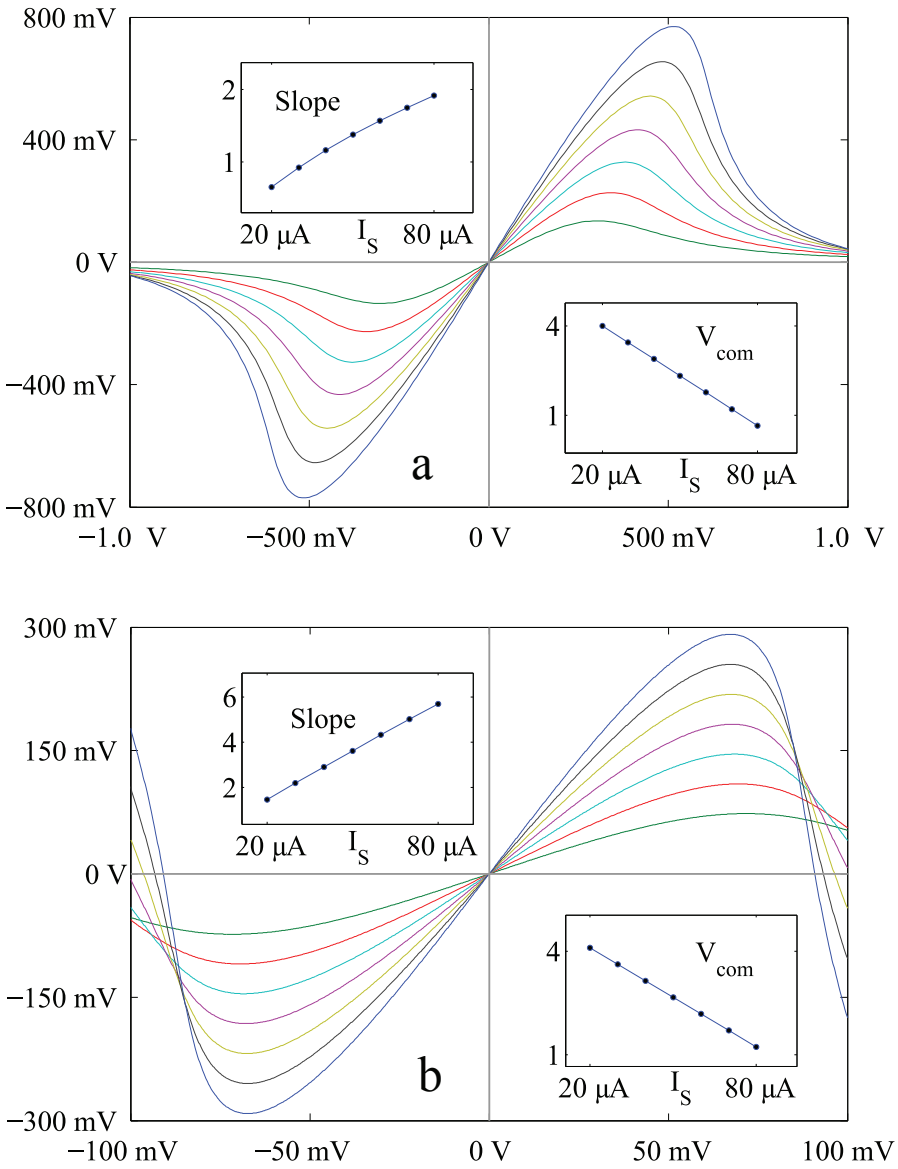


Figure 3.4 – Differential input-output voltage transfer curves obtained from Verilog-A / Cadence Spectre simulations for different values of I_S, ranging from 20 µA to 80 µA in steps of 20 µA; The insets on the top left show the slope (voltage gain) at $V_{in} = 0$ for each value of I_S. The insets on the bottom right show the value of V_{com} which were used for the respective bias current level. The device parameters were (a) $g_m = 100\mu S/V$, $g_0 = 50\mu S$, (b) $g_m = 400\mu S/V$, $g_0 = 40\mu S$. In both cases $V_{DD} = 5V$, $V_0 = 0$, $R_L = 3(1/g_0)$ and the contact resistance at source and drain were $R_C = 1k\Omega$.

can significantly boost our differential circuit's performance (figure 3.4b). We extracted the characteristics from I(V) curves of bilayer graphene devices presented in reference [84], where the values of g_m and g_0 were found to be on the order of 400 µS/V and 40 µS respectively (at $V_{bg} = -80V$). The low base conductance is due the band gap opening in bilayer graphene when applying an electric field via a back gate bias V_{bg}. However, as mentioned above, the price to pay for the higher voltage gain is a drastically reduced input swing.

3.5 Conclusion

We studied the behavior of a proposed differential circuit that could be an alternative to the traditional CMOS paradigm. The results show a useful operation region with higher than unitary slope, which is notoriously difficult to achieve with graphene-based devices, indicating that cascading of such differential blocks should be feasible.

The simple empirical device model established at the beginning of this chapter allowed us to analytically calculate the circuit's behavior, giving us qualitative insight into the characteristics of the transfer function. This insight enabled us to tune the bias conditions, notably V_{com}, in order to optimize the circuit's operating performance, maximizing the slope of its transfer function. The circuit was then numerically modeled by implementing an empirical model in Verilog-AMS and running it in a circuit simulator.

Despite the encouraging results, we also have to note some limitations inherent to the here considered graphene device technology. The initial goal in the circuit design was to overcome the handicap stemming from the modest on-off ratios expected in graphene transistors. It turns out that a similar limitation, the ratio between transconductance and base conductance g'_m/g_0, also affects the performance of the proposed differential graphene circuit.

4 A Physical Device Model

Throughout most of the work described in this thesis, including data analysis, analytical calculations and circuit simulation, the graphene devices were described using empirical models. Although the more advanced models were able to fit and capture the measured device characteristics extremely well, it remains interesting to better understand the physical background and possibly reconcile some of the fitting parameters, such as transconductance and base conductance, with actual physical quantities.

Champlain [172] derived the behavior of the graphene field effect device in a very comprehensive first-principles theoretical examination. Carrier concentrations are calculated as the exact solution of the Fermi-Dirac integral from the linear density of states. A rigorous charge-voltage relation is established, relating the bias voltages at the device terminals with the amount of charge inside the graphene channel and the local Fermi level relative to the Dirac point.

This charge-voltage relation, however, is found to be transcendental, notably because the Boltzmann approximation cannot be made in the case of graphene, allowing no closed-form solution. Consequently, all further computations rely on a numerical solution of this equation, solving it for η_F the normalized Fermi level. Once η_F is known, the complete current-voltage characteristic of the device can be exactly derived.

In this chapter, we show that the charge-voltage relation can be transformed into a simple quadratic equation with two analytical solutions, by replacing exact (polylogarithmic) carrier density with its asymptotic approximation. These asymptotic solutions can then be "extended" such that they provide a highly accurate solution for the entire range of bias conditions.

4.1 Carrier Statistics in Graphene

Compared to Silicon, there are two major differences in the way carrier concentrations have to be calculated. In (nondegenerate) Silicon, the Fermi level is located inside the band gap where the density of states is zero. Outside the band gap, the Fermi-Dirac distribution can well be approximated with the Boltzmann distribution. This is not true in the case of graphene where no band gap exists and capturing the exact value of the carrier concentration close to the Dirac point is essential. Secondly, the density of states follows a square-root law whereas

in graphene it is approximately linear and can be written as[1]

$$D(E) = \frac{g_s g_v}{2\pi} \frac{|E - E_D|}{(\hbar v_F)^2} \tag{4.1}$$

where g_s and g_v are the spin and valley degeneracies, $\hbar$ is the reduced Plank's constant, v_F is the Fermi velocity and E_D the energy at the Dirac point.

The carrier concentrations are obtained by integrating the product of the density of states (DOS) with the Fermi-Dirac distribution as follows

$$n = \int_{E_D}^{\infty} D(E) f(E)\, \mathrm{d}E \qquad\qquad p = \int_{-\infty}^{E_D} D(E) \bar{f}(E)\, \mathrm{d}E \tag{4.2 a,b}$$

where $\bar{f}(E) = 1 - f(E)$. The solution to Fermi-Dirac integrals can generally be expressed using the exponential function e^x and a polylogarithm Li_k [174]: $\mathcal{F}_k(x) = -Li_{k+1}(-e^x)$, where $\mathcal{F}_k$ is the Fermi-Dirac integral of order k. When describing traditional semiconductors with a parabolic band structure, half-integer polylogarithms are usually encountered. In the case of graphene, due to the linear DOS, the solution to equations (4.2) involves the second-order polylogarithm (details are given in appendix A.1). To simplify the notation, we define $\mathcal{L}_k(x) = -Li_k(-e^x)$.

$$n = N_G \mathcal{L}_2(\eta_F) \qquad\qquad p = N_G \mathcal{L}_2(-\eta_F) \tag{4.3 a,b}$$

N_G, the effective graphene density of states, is defined as

$$N_G = \frac{g_s g_v}{2\pi} \left(\frac{k_B T}{\hbar v_F} \right)^2 \tag{4.4}$$

where $g_s = g_v$ are the spin and valley degeneracies, $v_F = 10^6\,\mathrm{m/s}$ is the Fermi velocity in Graphene and $\hbar$ is the reduced Planck's constant. At room temperature ($T = 300\mathrm{K}$) the value of N_G is $9.8 \cdot 10^{10}\mathrm{cm}^{-2}$. The unitless parameter η_F is the reduced Fermi energy relative to the Dirac point:

$$\eta_F = \frac{E_F - E_D}{k_B T}. \tag{4.5}$$

The carrier statistics in graphene are thus governed by the $\mathcal{L}_2$-function, defined as the composition of the dilogarithm with the exponential function (the resulting concentrations are plotted in figure 4.1). For our modeling approach it is essential to understand the behavior of this function. Its transcendental nature is the reason why the charge voltage relation described in section 4.2, which is fundamental to the device analysis, cannot be solved explicitly.

In the left branch ($x < 0$), $\mathcal{L}_k$ behaves like the exponential function, regardless of the value of k. In terms of carriers, the electron concentration decays exponentially the more the

[1] The development in this section largely follows and expands on Champlain's first-principles examination[172].

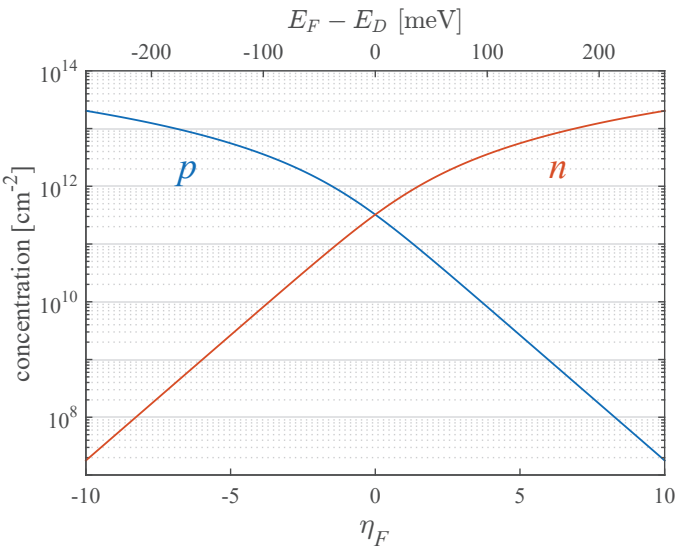


Figure 4.1 – Carrier concentrations as a function of the Fermi level relative to the Dirac point; normalized as η_F (bottom axis), and in actual units (top axis). At $\eta_F = 0$ the value of $\mathcal{L}_2(0) = \pi^2/12$ is close, but not exactly exactly equal to unity and $n(0) = p(0) = 0.82 \cdot N_G$, which amounts to $8.1 \cdot 10^{10}\,\mathrm{cm}^{-2}$.

Fermi level drops below the Dirac point ($\eta_F < 0$). This corresponds to the familiar Boltzmann approximation made in non-degenerate semiconductor materials. In the right branch, where ($x > 0$), $\mathcal{L}_k(x)$ behaves like a polynomial of order k. For example, $\mathcal{L}_1$ shows linear behavior while $\mathcal{L}_2$, which represents the majority carrier concentration, resembles a parabola.

There are two important quantities to consider in the analysis of the graphene channel: the total concentration of carriers $n + p$ and the net charge concentration $p - n$. Their reduced counterparts, normalized by N_G, are $\mathcal{G}_2(\eta_F) = \mathcal{L}_2(\eta_F) + \mathcal{L}_2(-\eta_F)$ and $\mathcal{H}_2(\eta_F) = \mathcal{L}_2(-\eta_F) - \mathcal{L}_2(\eta_F)$, respectively. In both these quantities the exponential branch is insignificant and the concentrations of charge and carriers are dominated by the polynomial nature of the $\mathcal{L}_2$-function, with the exception of the transition region in the vicinity of the Dirac point.

In the case of total carrier concentration there is an exact identity

$$\mathcal{L}_2(\eta_F) + \mathcal{L}_2(-\eta_F) = \frac{\pi^2}{6} + \frac{1}{2}x^2, \tag{4.6}$$

whereas in the case of net charge there are two asymptotic limits

$$\mathcal{L}_2(-\eta_F) - \mathcal{L}_2(\eta_F) \approx \begin{cases} +\dfrac{\pi^2}{6} + \dfrac{1}{2}x^2, & \text{for } \eta_F \ll 0 \\ -\dfrac{\pi^2}{6} - \dfrac{1}{2}x^2, & \text{for } \eta_F \gg 0 \end{cases} \tag{4.7}$$

These relations will be helpful in solving the charge-voltage relation approximately by substituting the $\mathcal{L}$-function with a parabolic expression. More details on the asymptotic behavior

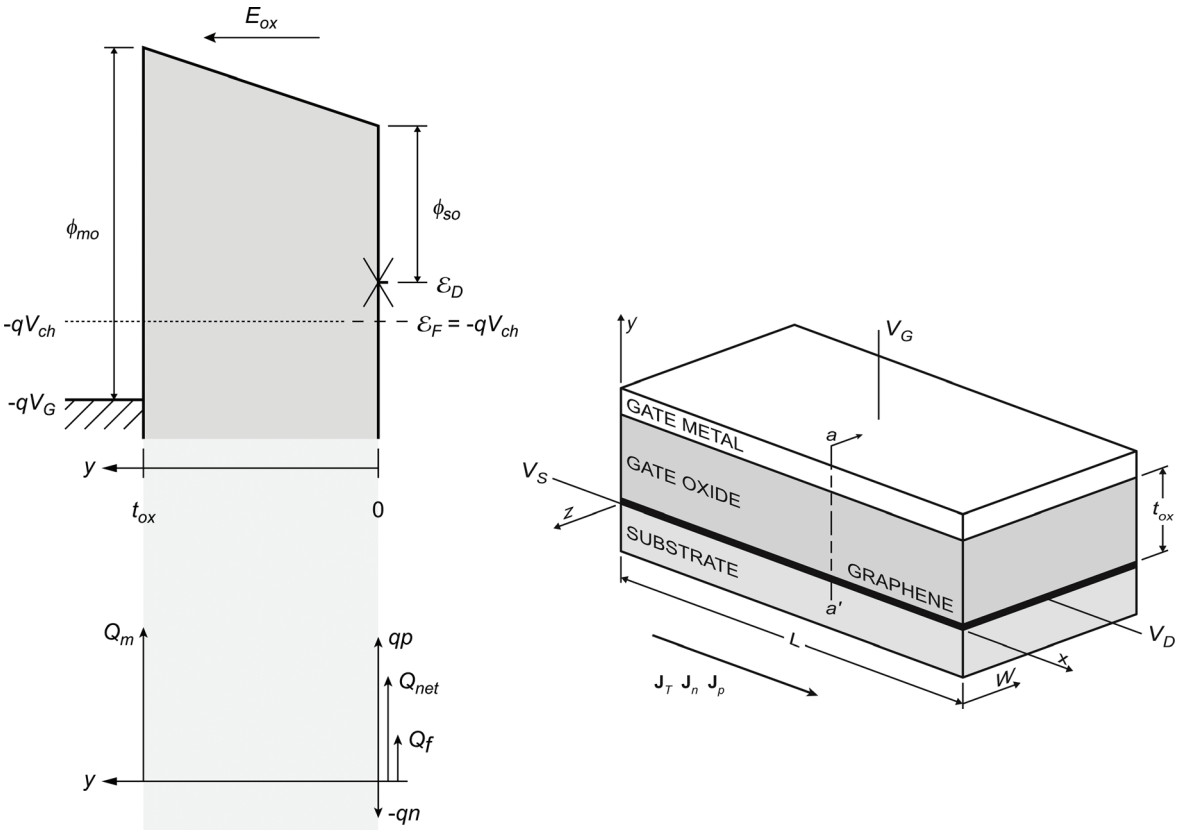


Figure 4.2 – Band Structure and charge profile of the gate cross-section (left) and perspective view of the substrate-channel-gate stack (right). The cross section left corresponds the dashed line $a - a'$ on the right. Graphic reprinted with permission from [172].

for the polylogarithm and $\mathcal{L}$-functions are provided in appendix A.2.

4.2 The Charge-Voltage Relation in a Graphene Transistor

The charge-voltage relation (4.8) relates the fermi level in the graphene sheet with the voltage applied to the transistor's gate electrode through the electrostatic interaction across the gate dielectric. The relation is derived by constructing a voltage loop, equating the potential drops across and on either side of the oxide, combined with the law of charge conservation. The details of this derivation can be found in reference [172]. In order to obtain charge and carrier concentrations as a function of the applied voltages, this equation first has to be solved for η_F.

$$V_G - V_{ch} + \frac{Q_{net}}{C_{ox}} - \frac{k_B T}{q}\eta_F + \frac{Q_f}{C_{ox}} - \frac{1}{q}\phi_{\mathrm{mo}} - \phi_{\mathrm{so}} = 0 \tag{4.8}$$

Here, V_G is the applied gate voltage, $V_{ch} = -E_F/q$ is the local voltage in the graphene channel, $Q_{\mathrm{net}} = q(p-n)$ is the net charge density, $C_{ox} = \varepsilon_{\mathrm{ox}}/t_{ox}$ is the areal gate oxide capacitance,

Q_f is the fixed charges density and ϕ_{mo} and ϕ_{so} are the metal-oxide and graphene-oxide workfunction differences, respectively.

First, we rearrange the equation, moving Q_{net} to the other side of the equals sign, and dividing by q. Either side of the equation has now the dimension of a density per unit area (cm^{-2}):

$$p - n = \frac{C_{ox}}{q}\frac{k_B T}{q}\eta_F - \frac{C_{ox}}{q}(V_G - V_{ch}) - \frac{Q_f}{q} + \frac{C_{ox}}{q}\left(\phi_{mo} - \phi_{so}\right) \tag{4.9}$$

By dividing both sides by N_G, we can normalize the equation and single out the transcendental functions on the left side of the equation. We use the normalized charge imbalance function $\mathcal{H}_2(\eta_F) = p' - n'$, defined in section 4.1, where $n' = n/N_G$ and $p' = p/N_G$ are the normalized carrier concentrations.

$$\mathcal{H}_2(\eta_F) = \frac{C_{ox}k_B T}{q^2 N_G}\eta_F - \frac{C_{ox}}{qN_G}(V_G - V_{ch}) - \frac{2Q_f}{qN_G} + \frac{2C_{ox}}{q^2 N_G}\left(\phi_{mo} - \phi_{so}\right) \tag{4.10}$$

At this point we can identify the dimensionless parameters a and b as well as the voltages V and V_0, which will simplify further developments.

$$a = \frac{1}{N_G}\frac{C_{ox}}{q}V_T \qquad b = \frac{1}{N_G}\frac{C_{ox}}{q}(V - V_0) \tag{4.11,12}$$

$$V = V_G - V_{ch} \qquad V_0 = \frac{\phi_{mo} - \phi_{so}}{q} - \frac{Q_F}{C_{ox}} \tag{4.13,14}$$

We can also define the two additional dimensionless symbols b' and v for later use, such that $b = b'v$:

$$b' = \frac{1}{N_G}\frac{C_{ox}}{q}V_T \qquad v = \frac{V - V_0}{V_T} \tag{4.15,16}$$

Substituting these symbols in equation 4.10 yields:

$$\mathcal{H}_2(\eta_F) = a\eta_F - b \tag{4.17}$$

The goal is to solve this equation and express η_F as a function of V. In other words, to find a relation between the bias conditions – the voltages at source, drain and gate – and the Fermi level inside the graphene channel. Once this relation is known, the carrier concentrations, which are directly dependent on η_F via eq. (4.3) can also be expressed as a function of V. Although equation (4.17) is transcendental due to the presence of the dilogarithm, it can be solved separately for different regions. The solutions are given in table 4.1.

In regions I and II, $\mathcal{H}_2$ is approximated by the parabola (A.16a,c) with a constant offset $\pm\pi^2/6$ from zero. In these cases, (4.17) becomes a simple, second-order equation and the solutions (4.19) exhibit a square-root like characteristic. The term $\pi^2/3$ in the square root, however, is problematic as it can lead the expression to assume imaginary values, even if b is constrained

	Region I	Region II	Region III	
	$x \ll 0$	$x \approx 0$	$x \gg 0$	
$\mathcal{H}_2(x)$	$\frac{1}{2}x^2 + \frac{\pi^2}{6}$	$x\log(4)$	$-\frac{1}{2}x^2 - \frac{\pi^2}{6}$	(4.18 a-c)
$\hat{\eta}_F$	$a - \sqrt{a^2 - \frac{\pi^2}{3} - 2b}$	$\frac{b}{a+\log 4}$	$-a + \sqrt{a^2 - \frac{\pi^2}{3} + 2b}$	(4.19 a-c)
$\tilde{\eta}_F$	$a - \sqrt{a^2 - 2b}$	$\frac{b}{a+\log 4}$	$-a + \sqrt{a^2 + 2b}$	(4.20 a-c)

Table 4.1 – Asymptotic solutions of the equation $\mathcal{G}(x) = ax - b$.

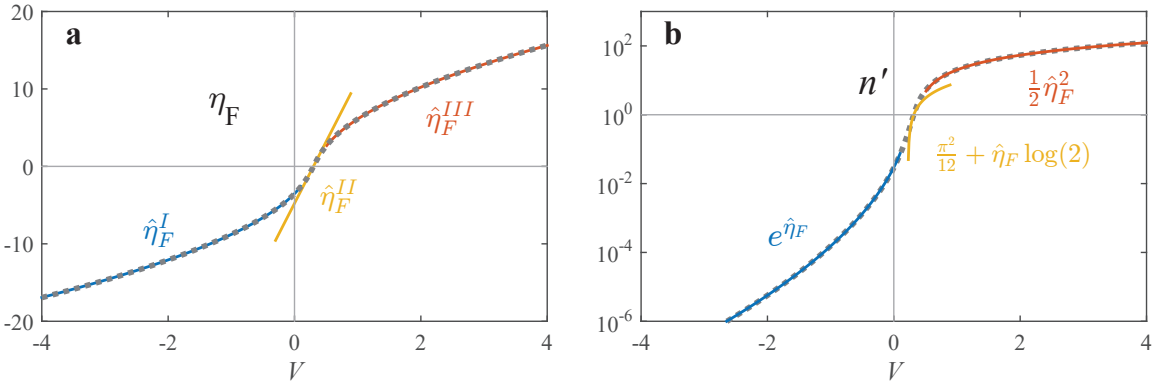


Figure 4.3 – Segment-wise asymptotic solutions of equation (4.17) (solid lines) as obtained from plotting (4.19) overlaid on the exact numerical solution (dotted line) (a). Segment-wise plot of the normalized carrier concentration, as obtained by substituting the asymptotic solutions (4.19) of the charge voltage relation (4.17) into $\mathcal{L}_2(x)$, overlaid on the exact numerical solution (dotted line) (b).

to non-negative numbers. Therefore, we also consider the reduced solutions (4.20), obtained by removing the constant term in (A.15a) and (A.15c). These reduced solutions are more convenient to use, give more accurate results in practice and have the distinct advantage of becoming zero: $\tilde{\eta}_F = 0$ for $b = 0$. In region II, we use the linearized form of $\mathcal{H}_2(x)$ at $x = 0$, leading to (4.17) becoming first order equation, which is straightforward to solve.

The curves resulting from this segment-wise approach are plotted in figure 4.3 together with the exact numerical result obtained from solving equation (4.8) using a nonlinear solver. The center point is shifted with respect to the origin $V = 0$ by $V_0 = 0.3\,\mathrm{V}$ as a result of the work-function difference $\phi_{\mathrm{mo}} - \phi_{\mathrm{so}} = 0.3\,\mathrm{eV}$ (the fixed charge density Q_{f} is chosen to be 0 here). The other relevant parameters are temperature ($T = 300\,\mathrm{K}$) and the oxide thickness ($t_{ox} = 15\,\mathrm{nm}$) and permittivity ($\varepsilon_{\mathrm{ox}} = 10\varepsilon_0$).

4.3 Pseudo-Fermi Levels

In the previous sections we have seen how the charge-voltage relation can be solved analytically if the dilogarithm-expression $\mathcal{L}_2(\eta_F)$ is replaced by its asymptotic approximation. Solving the equation is possible because the approximation is a second degree polynomial, but it only leads to segment-wise solutions each valid in the region where the corresponding asymptotic limit is applicable.

In the following approach, we re-formulate the charge-voltage relation using a newly defined set of variables. This will allow to solve the equation separately for electrons and holes over the full voltage domain range. Firstly, $\mathcal{L}_2(\eta_F)$ and $\mathcal{L}_2(-\eta_F)$ are each replaced with a variable that reflects the parabolic nature of $\mathcal{L}_2$ as given by equations (4.18 a,c).

$$\eta_n = \sqrt{2\mathcal{L}_2(+\eta_F)} \qquad\qquad \eta_p = -\sqrt{2\mathcal{L}_2(-\eta_F)}. \tag{4.21 a,b}$$

With this particular definition of η_n and η_p, the following relations are analytically exact and by substituting (4.21) into (4.22) one retrieves equation (4.3):

$$n' = \frac{1}{2}\eta_n^2 \qquad\qquad p' = \frac{1}{2}\eta_p^2 \tag{4.22 a,b}$$

One might refer to these quantities, η_n and η_p as *pseudo*-Fermi levels for electrons and holes, which should not be confused with the *quasi*-Fermi levels routinely used to describe carrier concentrations in semiconductors outside thermal equilibrium. Our pseudo-Fermi levels are a vehicle to simplify further algebraic manipulations and to emphasize the polynomial behavior of ensuing expressions. The comparison given in figure 4.4 reveals that η_n and η_p behave like *ramp functions* that constitute a decomposition of η_F into a left and a right branch. The sum of both pseudo-levels happens to equal $\eta_F \approx \eta_n + \eta_p$, except for a small, quantifiable error δ, plotted in figure 4.4b.

A charge-voltage relation can now be written separately for electrons and holes

$$-n' = a\eta_n - b_n \qquad\qquad p' = a\eta_p - b_p \tag{4.23 a,b}$$

where we have substituted the voltage-dependent variable $b(v) = b'v$ by the two ramp functions $b_n(v)$ and $b_p(v)$, which decompose $b(v)$ into a left and a right branch with respect to v, similarly to the decomposition of η_F into η_n and η_p. Equations (4.23) satisfy the charge-voltage relation (4.10) approximately since $\eta_n + \eta_p \approx \eta_F$ and the ramp functions are chosen such that $b_n + b_p = b$.

$$\begin{aligned} p' - n' &= a\left(\eta_n + \eta_p\right) - \left(b_n + b_p\right) \\ &= a\eta_F - b \end{aligned} \tag{4.24}$$

The partial charge-voltage relations for holes and electrons (4.23) can be written equivalently,

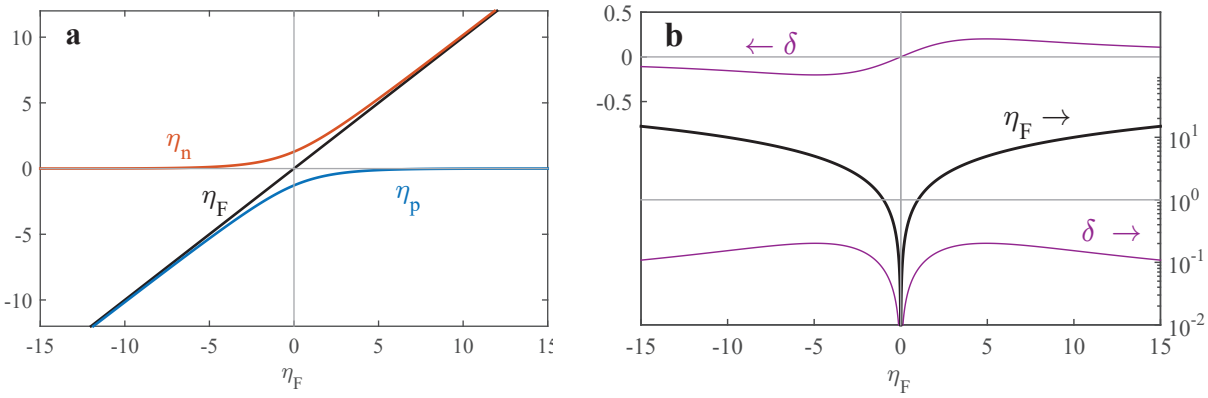


Figure 4.4 – Comparison of η_F and the pseudo Fermi levels η_n and η_p (a). Error δ between η_F and $\eta_n + \eta_p$ on a linear scale (left axis) and on a logarithmic scale compared with η_F, which is roughly two decades larger (right axis) (b).

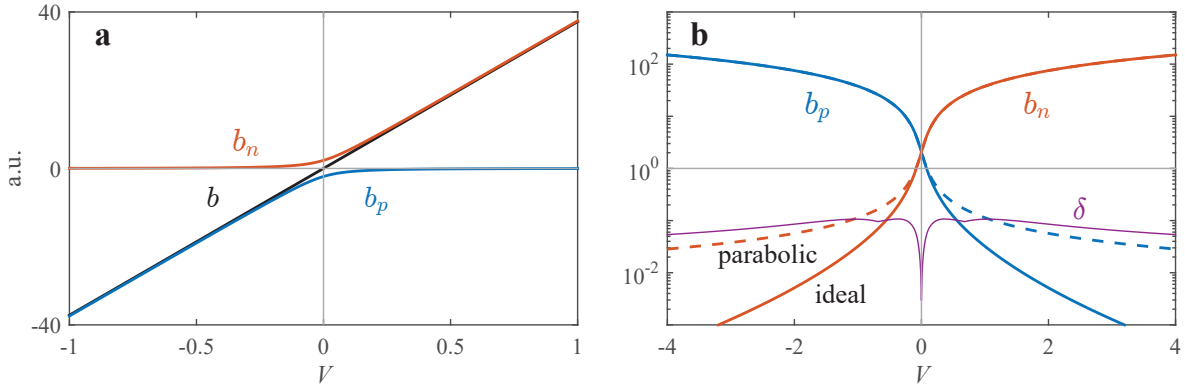


Figure 4.5 – Voltage ramp functions $b_n(v)$ and $b_p(v)$ versus $b(v) = b'v$ on linear scale (a) and logarithmic scale (b). In figure b, the solid lines represent the ideal voltage ramp, while the dashed lines are the parabolic ramp function.

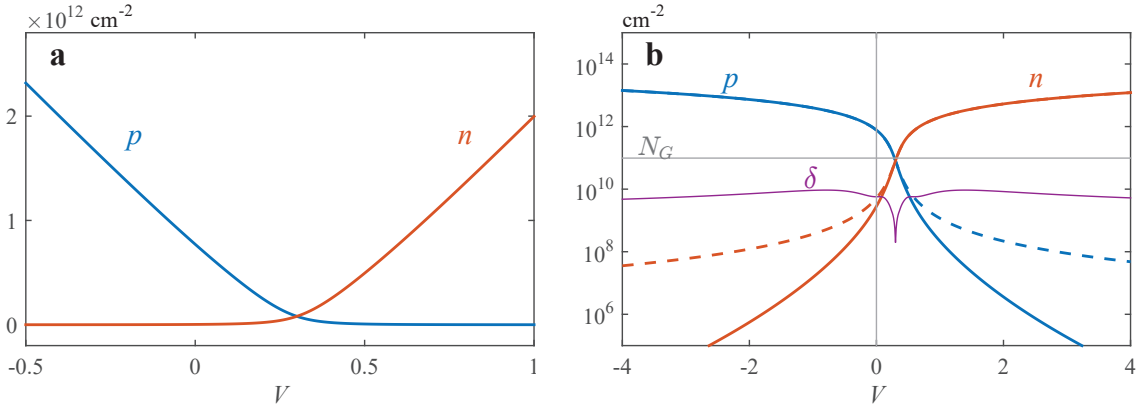


Figure 4.6 – Carrier concentrations as a function of voltage in linear (a) and logarithmic scale (b). The solid lines are the reference numeric solution whereas the dashed lines correspond to the result obtained using our model based on the pseudo-Fermi levels η_n, η_p and the parabolic ramp approximation of b_n, b_p.

using the definitions of η_n and η_p (4.22), as

$$-\frac{1}{2}\eta_n^2 = a\eta_n - b_n \qquad \frac{1}{2}\eta_p^2 = a\eta_n - b_p \tag{4.25 a,b}$$

leading to the solutions:

$$\eta_n = -a + \sqrt{a^2 + 2b_n} \qquad \eta_p = a - \sqrt{a^2 - 2b_p} \tag{4.26 a,b}$$

These equations (4.26) are the principal result of this work. All relevant quantities including carrier concentration, current and conductances can be expressed in terms of η_n and η_p as a function of voltage v. The functions b_n and b_p are plotted in figure 4.5. One can numerically determine an ideal voltage ramp, which, when plugged into equations (4.23), result in logarithmic accuracy of the carrier concentration. A closed-form expression for b_n and b_p, however, cannot be given for the same reason that η_F is not analytically solvable with respect to v.

The ideal voltage ramp can well be replaced with a parabolic ramp function discussed in appendix A.3. This approximation is very accurate in the linear branch but slightly deviates in the opposite branch, where it decays at a lower rate. By adjusting the ramp parameter α the ramp can be optimized to yield the exact result at the Dirac point $v = 0$. This ramp parameter adjustment is more extensively discussed in appendix A.4. The result can be seen in figure 4.6; on the linear scale, the numeric solution and the analytic approximation are indistinguishable. Note that in the majority branch, n and p appear to be linear with V. The carrier concentrations have a parabolic relation with the pseudo-Fermi levels (eq. 4.22) but the dependence of η_n, η_p on voltage is essentially a square-root law (eq. 4.26). These compensate, leading to a predominantly linear relation between n, p and V, although a smaller square-root component is still present (c.f. eq. A.36c and A.37a, appendix A.4).

4.4 Quantum Capacitance

The quantum capacitance, which has an impact on the device's characteristic near the Dirac point, is implicitly taken into account in this model. The definition of C_Q is

$$C_Q = \frac{q}{k_B T}\frac{\partial Q_{\text{net}}}{\partial \eta_F} = \frac{q}{k_B T}\frac{\partial}{\partial \eta_F} q(p - n). \tag{4.27}$$

C_Q can be computed by substituting $\mathcal{H}_2(\eta_F)$ as defined in section 4.1 into (4.27) and evaluating the derivative. Taking into account that $\frac{\mathrm{d}}{\mathrm{d}x}\mathcal{L}_2(\pm x) = \pm\mathcal{L}_1(\pm x)$ as well as $\mathcal{L}_1(\eta_F) = \log(1 + e^x)$ one obtains the following analytical expression:

$$C_Q = \frac{q^2 N_G}{k_B T}\left(\log(1 + e^{\eta_F}) + \log(1 + e^{-\eta_F})\right). \tag{4.28}$$

Figure 4.7 plots the normalized quantum capacitance (C'_Q) against the gate voltage, where $\hat{\eta}_F$ is directly numerically evaluated from (4.8) and plugged into (4.28). The dashed line is the

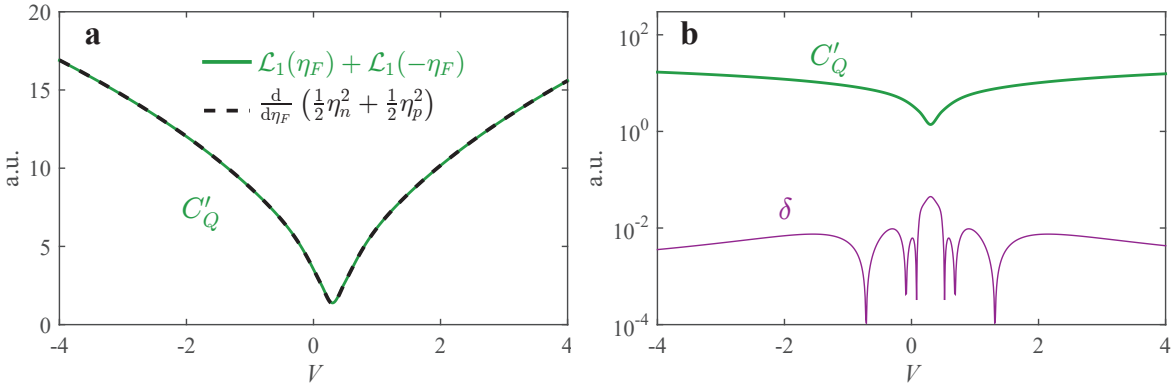


Figure 4.7 – Normalized quantum capacitance obtained from the analytical expression (4.28) (solid line) and by taking the derivative of the charge model (dashed line) (a). The absolute error δ between the model-based and the numerically determined quantum capacitance is at least two decades below C'_Q throughout most of the voltage domain.

sum of carriers obtained from the ramp-based carrier model (4.26), differentiated by the same $\hat{\eta}_F$. The curves are near-identical, confirming that (4.26) provides a good model for the carrier concentration and includes the effect of quantum capacitance.

4.5 Drift-Diffusion Current

To model transport as drift-diffusion currents in semiconductor devices, two separate quasi Fermi levels for the conduction and valence bands are commonly introduced, where the current density of each carrier type is proportional to the gradient of the corresponding quasi Fermi level. The reason is that by applying a bias to the device, electrons and holes are no longer in thermal equilibrium with each other. The carrier populations within a single band, however, are considered to be in equilibrium internally and can each be described with a separate Fermi level. Considering the zero band gap in graphene, the conduction and valence bands are assumed to be closely enough connected so that the difference between the quasi Fermi levels is minimal. Instead a single Fermi level is used here to model both electron and hole currents.

This approach is expected to be accurate for low source-drain bias voltages and a relatively weak longitudinal electric field in the channel. In that case near-equilibrium carrier populations are a probable situation. For higher V_{DS} and fields on the order of 1 V/µm or larger, carrier velocity saturation is likely to occur [175, 161]. At even larger fields, on the order of 2 V/µm or higher, the carrier populations are expected to be significantly increased due to the onset of high-energy carrier collisions [176, 177]. Graphene is particularly susceptible to this type of inter-band interaction, which is favored in semiconductors with small band gaps[178]. However, there is benefit in considering low bias conditions, as the most useful region of operation graphene field effect devices is where V_{DS} is smaller than the gate voltage.

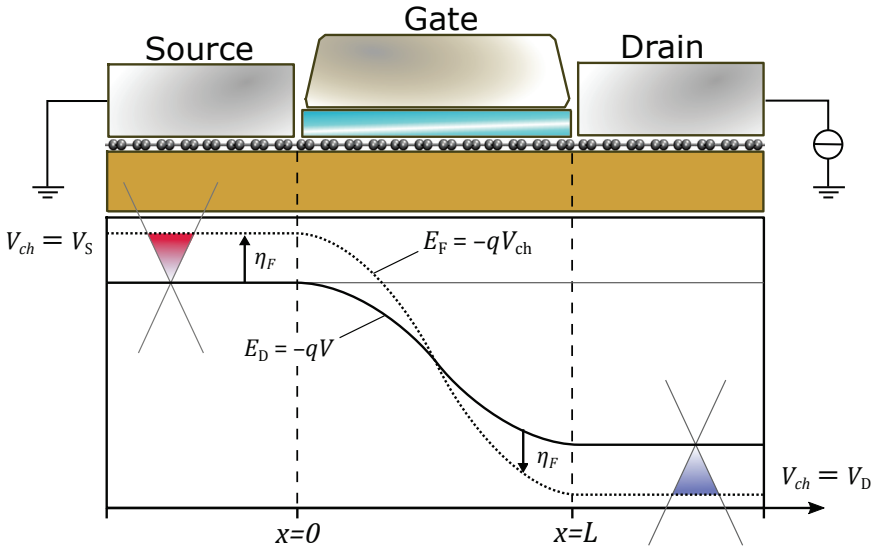


Figure 4.8 – Schematic illustrating the structure of the device under investigation. The top part shows the graphene sheet sandwiched between an insulating substrate and the source, drain and gate electrodes, the gate being separated from the channel by a thin dielectric. The lower part illustrates the band structure under a particular set of bias conditions. The dashed vertical lines separate the gated channel region from the contact regions.

Here, the current dependence on V_G is linear and g_m is highest, allowing to fully utilize the mobility-enabled large transconductance.

Figure 4.8 illustrates the device structure and the different variables that are relevant in evaluating the current. In the contact regions the channel voltage V_{ch} corresponds to the voltages applied to the source and drain terminals, V_S and V_D. The electrostatic potential E_D (solid line) corresponds to the Dirac level and η_F represents the offset between the Fermi level E_F (dotted line) and E_D and determines the local carrier concentration. In the particular situation depicted here, there is a crossover between the lines where $\eta_F = 0$, the total carrier concentration has a minimum and the electric field is at a peak. At the source (drain) side, to the left (right) of the crossover there is a majority-electron (hole) concentration, indicated by the red-shaded (blue) area in the Dirac cone. This situation occurs when the gate potential is between the source and drain potentials, and the device's output current is at or near its minimum, i.e. the Dirac point.

4.5.1 Drift Current

Drift current density is proportional to the electric field in the channel, which is the gradient of the electrostatic potential E_D.

$$\vec{J}_{n\,\mathrm{dft}} = qn\mu_n\vec{E} = -n\mu_n\nabla E_D \qquad \vec{J}_{p\,\mathrm{dft}} = qp\mu_p\vec{E} = -p\mu_p\nabla E_D \tag{4.29 a,b}$$

Recalling the definitions of $\eta_F = (E_F - E_D)/k_B T$ and $E_F = qV_{ch}$, the electrostatic potential can be expressed as $E_D = -qV_{ch} - k_B T\eta_F$. Using the definition of $\upsilon = (V_G - V_{ch} - V_0)/V_T$, one recognizes that $V_T \nabla \upsilon = \nabla V_{ch}$ because V_G and V_0 are constant throughout the channel. Thus, the gradient can be written in terms of the known variables υ and eta_F obtained from solving the charge-voltage relation:

$$\begin{aligned} -\frac{1}{q}\nabla E_D &= V_T \nabla \upsilon + \frac{k_B T}{q}\nabla \eta_F \\ &= V_T \left(\nabla \upsilon + \nabla \eta_F\right). \end{aligned} \tag{4.30}$$

Assuming a uniform channel throughout the width of the device, the problem can be reduced to a single dimension and the gradient replaced by $\frac{\mathrm{d}}{\mathrm{d}x}$, using x as the longitudinal axis. We can then evaluate the current in the usual way by moving the differentials $\mathrm{d}x$ to the left,

$$J_{n\mathrm{dft}}\,\mathrm{d}x = q\mu_n V_T \left(n\,\mathrm{d}\upsilon - n\,\mathrm{d}\eta_F\right) \qquad J_{p\mathrm{dft}}\,\mathrm{d}x = q\mu_p V_T \left(p\,\mathrm{d}\upsilon - p\,\mathrm{d}\eta_F\right) \tag{4.31 a,b}$$

and integrating from source to drain

$$\int_{x_S}^{x_D} J_{n\mathrm{dft}}\,\mathrm{d}x = q\mu_n V_T \int_{\upsilon_S}^{\upsilon_D} n\,\mathrm{d}\upsilon - q\mu_n V_T \int_{\eta_S}^{\eta_D} n\,\mathrm{d}\eta_F \tag{4.32a}$$

$$\int_{x_S}^{x_D} J_{p\mathrm{dft}}\,\mathrm{d}x = q\mu_p V_T \int_{\upsilon_S}^{\upsilon_D} p\,\mathrm{d}\upsilon - q\mu_p V_T \int_{\eta_S}^{\eta_D} p\,\mathrm{d}\eta_F \tag{4.32b}$$

where the integral limits correspond to position, voltage and reduced fermi level at the source and drain, respectively. Since we replaced the integration variable E_D by a combination of υ and η_F there are now two integral to solve for each carrier type.

4.5.2 Diffusion Current

Diffusion current density is proportional to the carrier concentration gradient, with diffusion coefficient D_n and D_p.

$$\vec{J}_{n\mathrm{dfn}} = qD_n \nabla n \qquad \vec{J}_{p\mathrm{dfn}} = qD_p \nabla p \tag{4.33 a,b}$$

Usually, the diffusion coefficients are replaced according to the Einstein relation $D = \mu k_B T$. This is, however, applicable only where carrier concentrations follow Boltzmann statistics. In graphene, the generalized Einstein relation has to be used:

$$D_n = \mu_n \frac{n}{q\frac{\mathrm{d}n}{\mathrm{d}E_F}} = \mu_n V_T \frac{n}{\frac{\mathrm{d}n}{\mathrm{d}\eta_F}} \tag{4.34}$$

The electron concentration gradient ∇n becomes $\frac{\mathrm{d}n}{\mathrm{d}x}$ for a 1-dimensional system, which can

be rewritten in terms of η_F:

$$\nabla n = \frac{\mathrm{d}n}{\mathrm{d}x} = \frac{\mathrm{d}n}{\mathrm{d}\eta_F}\frac{\mathrm{d}\eta_F}{\mathrm{d}x} \tag{4.35}$$

Plugging (4.35) into (4.33) leads to the following relation, where the $\mathrm{d}n$ and $\mathrm{d}\eta_F$ cancel out

$$J_{n\mathrm{dfn}} = qD_n\frac{\mathrm{d}n}{\mathrm{d}x} = q\mu_n V_T \frac{n}{\frac{\mathrm{d}n}{\mathrm{d}\eta_F}}\frac{\mathrm{d}n}{\mathrm{d}\eta_F}\frac{\mathrm{d}\eta_F}{\mathrm{d}x} \tag{4.36}$$

The development for holes is analogous, and after rearranging the differentials

$$J_{n\mathrm{dfn}}\,\mathrm{d}x = q\mu_n V_T n\,\mathrm{d}\eta_F \qquad\qquad J_{p\mathrm{dfn}}\,\mathrm{d}x = q\mu_p V_T p\,\mathrm{d}\eta_F \tag{4.37 a,b}$$

we can again define the integrals from source to drain:

$$\int_{x_S}^{x_D} J_{n\mathrm{dfn}}\,\mathrm{d}x = q\mu_n V_T \int_{\eta_S}^{\eta_D} n\,\mathrm{d}\eta_F \tag{4.38a}$$

$$\int_{x_S}^{x_D} J_{p\mathrm{dfn}}\,\mathrm{d}x = q\mu_p V_T \int_{\eta_S}^{\eta_D} p\,\mathrm{d}\eta_F \tag{4.38b}$$

4.5.3 Integration

Overall, there are two integrals that need to be evaluated:

$$\int n\,\mathrm{d}\eta_F \tag{4.39}$$

$$\int n\,\mathrm{d}v \tag{4.40}$$

We want to integrate the carrier concentration over v and over η_F. From the developments in section 4.3 we know how η_n and η_p depend on v and η_F, therefore it is possible to make a change of variable. In the case of (4.39) this change is quite straightforward if we replace n with $\frac{1}{2}\eta_n^2$ and $\mathrm{d}\eta_F$ with $\mathrm{d}\eta_n$:

$$\int n\,\mathrm{d}\eta_F \approx \int \frac{1}{2}\eta_n^2\,\mathrm{d}\eta_n = \frac{1}{6}\eta_n^3. \tag{4.41}$$

In the case of (4.40) the change of variable requires the addition of a term $\mathrm{d}v = \frac{1}{b'}\left(\eta_n + a\right)\mathrm{d}\eta_n$:

$$\int n\,\mathrm{d}v = \int \frac{1}{2}\eta_n^2\,\mathrm{d}v \approx \int \frac{1}{2}\eta_n^2\frac{1}{b'}\left(\eta_n + a\right)\mathrm{d}\eta_n. \tag{4.42}$$

resulting in a 3rd and a 4th-order term of η_n. Note that $a/b' = 1$ and cancel out.

$$\int \frac{1}{2}\eta_n^2\,\mathrm{d}v \approx \int \left(\frac{1}{2b'}\eta_n^3 + \frac{1}{2}\eta_n^2\right)\mathrm{d}\eta_n = \frac{1}{8b'}\eta_n^4 + \frac{1}{6}\eta_n^3 \tag{4.43}$$

Comparing the equations (4.32) and (4.38), one recognizes that diffusion current $\int n\,\mathrm{d}\eta_F$ is identical the second of the terms that make up drift current $\int n\,\mathrm{d}v - \int n\,\mathrm{d}\eta_F$. Taking the sum of drift and diffusion, this term cancels and the result is proportional to $\int n\,\mathrm{d}v$. Equation (4.43) thus represents the total drift + diffusion current, where the 3rd order term in (4.41) and (4.43) constitutes diffusion current and the 4th order term in (4.43) is the drift current.

The left side of equations (4.38) and (4.32) integrates the current density from source ($x_S = 0$) to drain ($x_D = L$). Dividing these integrals by the channel length L results in an average current $\bar{J}_n$ and $\bar{J}_p$ (the respective drift and diffusion components) and multiplying by the channel width W yields the corresponding currents I_n and I_p, assuming a channel that is uniform throughout its width.

Finally we get the drift components

$$I_{n\mathrm{dft}} = I_{n0}\frac{1}{8b'}\eta_n^4\Big|_{v_{gs}}^{v_{gd}} \qquad I_{p_{\mathrm{dft}}} = I_{p_0}\frac{1}{8b'}\eta_p^4\Big|_{v_{gs}}^{v_{gd}} \tag{4.44 a,b}$$

and the diffusion components

$$I_{n\mathrm{dfn}} = I_{n0}\frac{1}{6}\eta_n^3\Big|_{v_{gs}}^{v_{gd}} \qquad I_{p_{\mathrm{dfn}}} = I_{p_0}\frac{1}{6}\eta_p^3\Big|_{v_{gs}}^{v_{gd}} \tag{4.45 a,b}$$

where I_{0n} and I_{0p} are defined as follows

$$I_{n0} = \frac{W}{L}q\mu_n V_T N_G \qquad I_{p_0} = \frac{W}{L}q\mu_p V_T N_G \tag{4.46 a,b}$$

The expressions are evaluated by substituting for v_{gd} and v_{gs} the gate-drain and gate-source potential differences, respectively, normalized by dividing by the thermal voltage V_T. The pseudo-Fermi levels $\eta_n(v)$ and $\eta_p(v)$ are known functions of voltage as defined by equations (4.26).

4.6 Results

With equations (4.44-4.46), we have a complete set of explicit expressions that allow to directly compute the total current as a function of the potentials applied to the device's source, drain and gate terminals. The total current is obtained by adding the drift and diffusion components of the electron and hole currents which can each be individually computed. The result is plotted in figure 4.9, which shows the current-voltage characteristic as a function gate and drain voltage as well as the corresponding conductances.

We observe that the current-voltage characteristic has near-linear behavior in the case of the $I_D(V_G)$ relation (figure 4.9a) and a near-quadratic one for $I_D(V_D)$ (figure 4.9b), which manifests as quasi constant g_m and linear g_{ds} (figure 4.9 c & d). In section 4.3, it was mentioned that carrier concentration exhibits a linear dependence on voltage, e.g. electrons $n \sim \eta_n^2 \sim v$. Now we see that (electron) drift current is proportional to η_n^4, thus leading to the quadratic relation

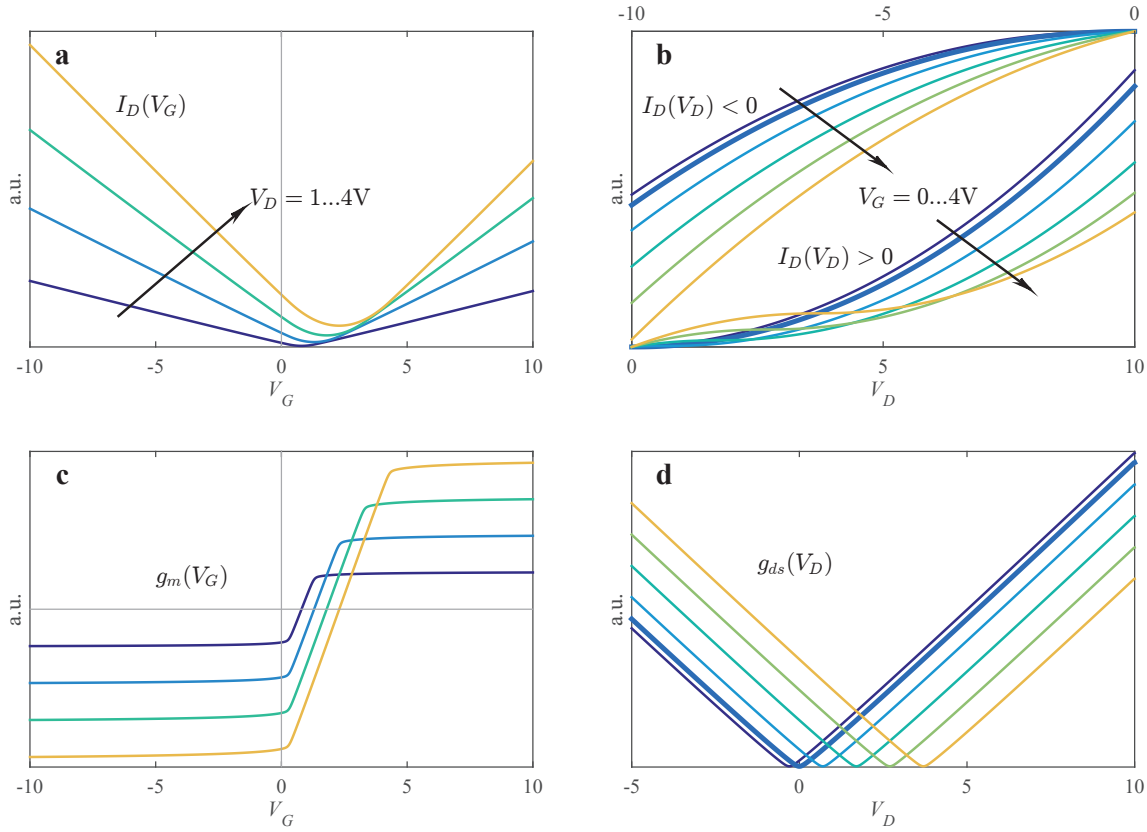


Figure 4.9 – Result (normalized) of the drift-diffusion current modeling. Drain current vs. gate voltage curves (a), drain current vs. drain voltage (b) transconductance vs. gate voltage (c) and drain-source conductance vs drain voltage (d). All voltages are referred to $V_S = 0$. The conductances g_m and g_{ds} are the derivatives of the $I_D(V_G)$ and $I_D(V_D)$ curves, respectively. The thick line in figures (b) and (d) corresponds to $V_G = V_0$.

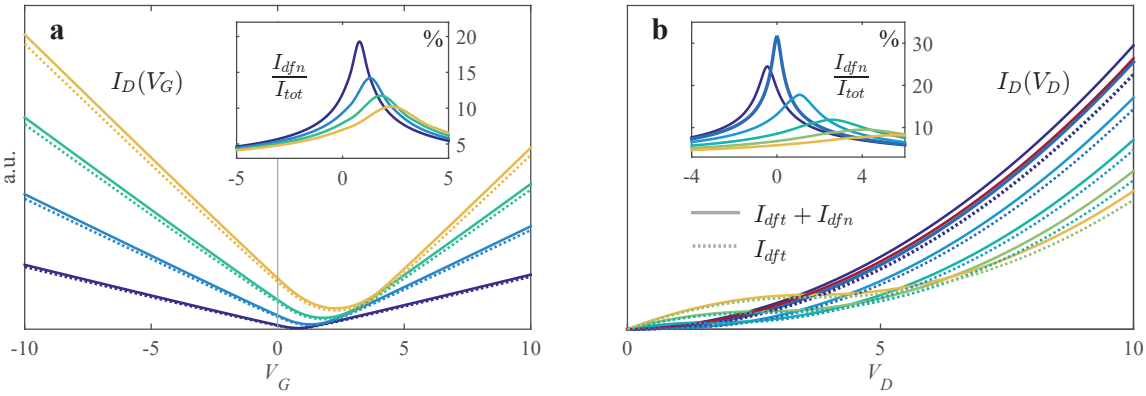


Figure 4.10 – Comparison of total (solid lines) and drift-only current (dotted lines) in the $I_D(V_G)$ (a) and $I_D(V_D)$ curves (b). The insets show the relative fraction of diffusion current in percent, which peaks at the Dirac point. The bias conditions are identical as in figure 4.9.

$i \sim v^2$, which we see in the $I_D(V_D)$ curves. The linear dependence on V_G shown in figure 4.9a is a result of how the drift current expressions (4.44) are evaluated at the limits v_{gs} and v_{gd} and can be explained by drawing a simplified picture: considering that $\eta_n^4 \sim v^2$ in the case of electrons, evaluating (4.44) amounts to computing the difference of v_{gd}^2 and v_{gs}^2 which expands to $(v_g - v_d)^2 - (v_g - v_s)^2$. In this last expression, the v_g^2-terms cancel out, leaving only first order terms of v_g, thus leading to the apparent linear relationship.

Between the linear branches left and right of the Dirac point in figure 4.9a, there is a region with parabolic current-voltage dependence and linear transconductance. The region is limited to where the gate potential falls between source and drain potentials $V_S < V_G - V_0 < V_D$. To take full advantage of graphene's mobility-enabled high transconductance, a device must be biased outside of this region, i.e. $V_G > V_{DS}$. The Dirac point itself, i.e. the global current minimum in the $I_D(V_G)$ relation, shifts with drain and source bias and is located at $\frac{1}{2}(V_D + V_S) + V_0$. This minimum translates into an inflection point in the $I_D(V_D)$ curves located where $V_D = V_G - V_0$ and channel conductance has a minimum with g_{ds} close to zero. This near-zero conductance may not be physical as it does not take into account the finite minimum conductivity discussed in section 1.4.2.

Since the current-voltage characteristic appears to be dominated by the $\eta_{n,p}^4$ terms, one could conclude that diffusion current plays only a subordinate role compared to drift current. Indeed, a comparison shows that drift current accounts for more than 90% of the total current, (figure 4.10) except in a region surrounding the Dirac point where diffusion current peaks at up to 30%.

We can assess the accuracy if this model by comparing its results with a reference model derived in appendix A.5. This reference current is computed by numerically solving the charge voltage relation for η_F, and then substituting that into the following expressions obtained

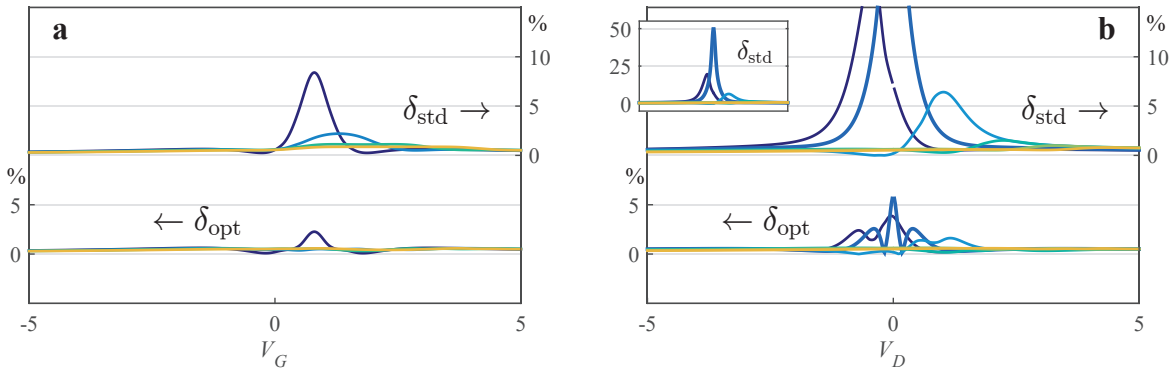


Figure 4.11 – Relative error, in percent, of the model (4.44)–(4.46) with standard (δ_{std}) and optimized (δ_{opt}) ramp parameter compared to the reference model (4.47). Figure (a) and (b) correspond to the $I_D(V_G)$ and $I_D(V_D)$ curves in figure 4.9, respectively, computed with identical bias conditions. The inset in figure b is provided for a full view of the δ_{std} curves. The extent of the horizontal axis is identical to that of the enclosing graph.

from integrating $n', p' = \mathcal{L}_2(\pm\eta_F)$ as described in appendix A.5:

$$i_{\text{ref,n}} = \mathcal{L}_3(\eta_F) \quad + \frac{1}{b'}\left(\mathcal{L}_2(\eta_F)^2 - \eta_F\mathcal{L}_3(\eta_F) + \mathcal{L}_4(\eta_F)\right) \tag{4.47a}$$

$$i_{\text{ref,p}} = \mathcal{L}_3(-\eta_F) + \frac{1}{b'}\left(\mathcal{L}_2(-\eta_F)^2 + \eta_F\mathcal{L}_3(-\eta_F) + \mathcal{L}_4(-\eta_F)\right) \tag{4.47b}$$

The elementary currents i are to be evaluated as $I = I_0 i\big|_{v_{gs}}^{v_{gd}}$ to obtain the effective current. Figure 4.11 illustrates the relative error of our model compared with the reference model. Two sets of curves are presented: The error δ_{std} corresponds to the case of simple standard ramp parameter adjustment (equal for all terms of $\eta_{n,p}$), whereas δ_{opt} corresponds to an optimized model where ramp parameters are adjusted to match the exact values of (4.47), term by term. The error is generally well below 1% everywhere except for the notorious region surrounding the Dirac point. In that region, the optimized ramp adjustment helps to substantially mitigate the error containing it below 6% at its peak. Note that this is despite the tendency of the relative error to become very large as the absolute value approaches zero, which is true in particular for the zero-crossing $I_D(V_D)$ curves at $V_D = 0$.

4.7 Conclusion

In conclusion, we modeled the carrier statistics in a graphene field-effect device following a rigorous approach based on Champlain's first-principles theoretical examination [172]. The electrostatic control of carriers inside the channel by an applied gate bias voltage is established through the charge-voltage relation which also implicitly accounts for the often neglected effect of quantum capacitance. We obtained a highly accurate approximations by studying the asymptotic behavior of the net charge concentration and solutions to the charge-voltage relation. Finally we were able to establish closed-form analytical expressions modeling charge

concentration and current directly as a function of the bias conditions applied to the device's terminals.

We find that various forms of ramp functions play a fundamental role in graphene analysis but also in the analysis of semiconductors in general. Ramps are not only a straightforward way to empirically describe the behavior of graphene devices, as shown in chapter 2. They also naturally occur in the form of the $\mathcal{L}_k$-functions as the solution to the Fermi-Dirac integral. While these functions, essentially variants of the exponential ramp function, are somewhat unwieldy when they occur in an equation to be solved, one can take advantage of their partially polynomial-like behavior. In our approach, we made use of pseudo-Fermi levels defined such that carrier statistics and current can be represented by simple exponentiation of these variables to the second, third and fourth power. In other words, we represent those quantities by polynomial expressions of the pseudo-Fermi levels. These are, in turn, modeled using parabolic ramp functions that very closely approximate the solution to the charge-voltage relation governed by the 2nd order exponential ramp function $\mathcal{L}_2$.

One of the strengths of this model is that drift, diffusion, electron and hole currents can individually computed. For example, by modeling the electron and hole current separately, different values of carrier mobilities can taken into account. Isolating drift and diffusion currents is also interesting as it sheds light onto their relative contribution to the total current and allows to estimate the potential error arising when only drift current is considered. The model could be extended or modified by taking other transport mechanisms into account, considering that drift-diffusion might not be the best means of describing current in graphene under all conditions. Finally, the model is continuous and valid for all combinations of gate, source and drain voltages without the need for artificial stitching functions, making it suitable for implementation as a compact model.

5 Conclusions

The present manuscript offers an examination of graphene, the first two-dimensional material ever discovered, and its properties from an electronic device point of view. The suitability and behavior of graphene-based electronic devices, in particular a field modulated transistor-like structure, is studied from different perspectives, including both practical-experimental and theoretical.

Chpater 1 gives a general overview of graphene and its applications. We see how the material (lattice) structure translates into a peculiar linear energy dispersion, making it a material class of its own, which is neither metallic-conducting nor a semiconductor. This results in both phenomenal electron mobility and very poor switching performance due to the lack of band gap, preventing the complete current turn-off which is necessary for logic electronics as we know it. Similar reasons also limit its use as a channel material in RF transistors. On the other hand, some advantages also come from its nature of being an atomically flat material. Those make it interesting in particular for flexible electronics but also applications where its surface to volume ratio can be leveraged to boost performance of batteries and capacitors.

Although graphene might not be suited as a direct replacement for current materials in today's semiconductor manufacturing processes, its outstanding properties are still likely to find applications in future electronics technologies. Those applications might be realized in novel devices, utilizing the various physical phenomena that occur in graphene, or take advantage of combinations with other 2D or bulk materials. Alternatively graphene could be used in new circuit architectures that depart from the currently dominating CMOS switching paradigm, such as the differential circuit approach we examine in chapter 3.

In chapter 2 we present details of a comprehensive examination of the graphene field effect device covering its design, fabrication, characterization and analysis. Establishing from scratch a workflow for this new technology, which had not been previously utilized in the research group, we introduce a set of coordinated tools, concepts and procedures which are optimized for efficiency, repeatability and incremental improvement.

We show how the fabrication process flow, specifically developed for graphene devices, takes into account the intricacies of graphene, including the delicacy of mechanical handling or its susceptibility to various processes and to contamination. The process uses electron beam

lithography, a very powerful, high resolution patterning technology, while avoiding direct exposure of essential device regions to electron beam radiation, which could incur significant damage to the graphene lattice. The process is also designed to prevent the graphene layer from coming into contact with plasma-based processes by ensuring that it is constantly protected by a oxide layer. This same layer also protects from contamination and facilitates the removal of organic residues after lithography, by allowing the use of highly effective plasma ashing.

From concept over realization to analysis, every stage is carefully embedded into the overall workflow with a toolset of instruments, procedures, concepts and software tools on each level. It begins with the prerequisite for device manufacturing: a powerful layout design framework, which its automated, has a highly modular and flexible operating principle and does not require any expensive software to be purchased. This framework is great for iterative design and incremental improvement, where changes are realized by adjusting a few lines of code, and can be easily integrated with a versioning control system such as GIT.

Along with the layout we simultaneously create the meta-information file that is later used to enable automated characterization. The automated/programmatic layout generation ensures that every device is charted with the right parameters at the right coordinates. This allows the electrical testing system to be aware of each device's location, type and properties while performing the measurements. Finally, at the last stage during data analysis, the same per-device information is available, where it can be used for structuring, grouping and sorting the measurement data, as well as to cross-reference and correlate it with respective device parameters. This workflow toolchain was created for, but is not limited to graphene devices and can be adapted for different needs.

In chapter 3 we see how the simple, empirical model can be used in hand calculations to make useful predictions of the behavior of a graphene-based circuit block. Further, we developed a circuit simulation environment that combines the strength of an industrial-grade SPICE simulator, incorporating the capabilities of verilog-A, with the versatility of MATLAB for data analysis and visualization. Our empirical graphene field-effect device model with closed-form expressions is well suited in this context, requiring only little computation time and consistently leading to converging solutions. The MATLAB-based front-end, used for managing source files, launching the simulation and loading the results back for further analysis and visualization, makes the process effective and convenient, allowing to readily improve and optimize circuit design and parameters.

We applied the principle of source-coupled logic to graphene, using the simulation environment to test numerous variants and optimize an elementary circuit block. To ensure realistic results, we simulated graphene-devices with parameters based on the performance and typical values from devices that were previously fabricated and characterized. However, we find that even in this alternative circuit design approach, and using optimistic parameter values, it is difficult to achieve high voltage gain, the main figure of performance of the circuit block. This limitation stems from the low ratio of transconductance, where a very high value is desirable, and base conductance, which should be as low as possible and corresponds to the notoriously

high off current in graphene. Voltage gain is necessary for cascading these circuit bloks and building circuits out of them.

The graphene circuit simulation environment remains useful however and is a powerful tool to study the behavior of graphene devices as components of a circuit. The empirical model has proven useful but one cannot rule out any doubt about its validity under all circumstances. Therefore it is interesting to compare it with a more rigorous model, both to confirm its validity and also to reconcile the circuit-level parameters with fundamental physical quantities.

From this perspective we developed a model based on asymptotic approximations of Champlain's rigorous description of the graphene field-effect device based on first principles. Using this approach we managed to find closed-form solutions to a normally transcendental problem. At the current stage the result can be considered zero-level model, providing valuable insight into the intrinsic behavior of graphene devices. However, it only takes ideal circumstances into account, excluding effects like velocity saturation, parasitic elements, noise etc. Such effects could certainly be incorporated in future extension of the model. The explicit analytical formulations and the absence of artificial elements such as step functions make it suitable for implementation as a compact model for accurate and effective circuit simulation.

In summary, we give a comprehensive picture centered on the graphene field-effect device from a practical, circuit-oriented standpoint, yet incorporating several different perspectives and approaches. These include the design and manufacturing of devices, an examination of their behavior and usefulness as circuit elements as well the theoretical study of physical laws that govern their functioning. Throughout the journey of exploring these perspectives we also developed a extensive collection of tools and procedures designed for graphene devices extensible to any type of electronic devices.

A Device Modeling Supplemental Information

A.1 Detailed Derivation of the Fermi-Dirac Integral

The product of the density of states $D(E)$ in graphene with the Fermi-Dirac distribution $f(E)$ defines the carrier occupancy and reads:

$$D(E)f(E) = \frac{g_s g_v}{2\pi} \frac{E - E_D}{(\hbar v_F)^2} \frac{1}{1 + e^{\frac{E-E_F}{k_B T}}} \tag{A.1}$$

The electron concentration is obtained by integrating this expression from E_D to $+\infty$. Here, a term $k_B T$ is added to make the the integrand more coherent.

$$n = \frac{g_s g_v}{2\pi} \frac{k_B T}{(\hbar v_F)^2} \int_{E_D}^{\infty} \frac{\frac{E-E_D}{k_B T}}{1 + e^{\frac{E-E_F}{k_B T}}} \, \mathrm{d}E. \tag{A.2}$$

In order to simplify this equation we can define normalized energies, centered around the dirac point E_D:

$$\eta_F = \frac{E_F - E_D}{k_B T} \qquad \eta = \frac{E - E_D}{k_B T} \qquad \eta - \eta_F = \frac{E - E_F}{k_B T} \tag{A.3}$$

By applying the change of variable

$$dE = \frac{dE}{d\eta} d\eta = k_B T \, \mathrm{d}\eta \tag{A.4}$$

the integral can be rewritten as

$$n = N_G \int_0^{\infty} \frac{\eta}{1 + e^{\eta - \eta_F}} \, \mathrm{d}\eta = N_G \mathcal{F}_1(\eta_F) \tag{A.5}$$

where $\mathcal{F}_1$ is the complete Fermi–Dirac integral with index $j = 1$, defined as

$$\begin{aligned}\mathcal{F}_j(x) &= \frac{1}{\Gamma(j+1)} \int_0^\infty \frac{t^j}{1+e^{t-x}} dt \\ &= -Li_{j+1}(-e^x).\end{aligned} \tag{A.6}$$

The function $Li_j(x)$ in the solution of this integral is known as the polylogarithm function.

$$Li_j(x) = \sum_{k=1}^{\infty} \frac{x^k}{k^j} = x + \frac{x^2}{2^j} + \frac{x^3}{3^j} + \ldots \tag{A.7}$$

In the case of graphene, as a consequence of the linear density of states, the relevant Fermi–Dirac integral has index $j = 1$, and accordingly, the carrier concentrations can be expressed using the polylogarithm of order 2, which is also called the dilogarithm function.

$$n = -N_G Li_2(-e^{\eta_F}) \tag{A.8a}$$

$$p = -N_G Li_2(-e^{-\eta_F}) \tag{A.8b}$$

Voilà.

A.2 Asymptotic behavior of charge- and carrier concentrations

Charge and carrier concentrations in graphene are governed by $\mathcal{L}_2$, which is composed the of the dilogarithm and the exponential function $\mathcal{L}_2(x) = -Li_2(y) = -Li_2(-e^x)$. It is useful to distinguish three regions, the left branch $x \ll 0$, the right branch $x \gg 0$ and where x is close to zero. The dilogarithm is real-valued for real values of $x \leq 1$, assumes positive values for $0 < x \leq 1$, zero for $x = 0$ and negative values for $x < 0$. With regard to the study of $\mathcal{L}_2$, the relevant domain of Li_2 is the range of $-e^x$, i.e. all negative values.

For large positive x, the dilogarithm has the following asymptotic limit[179]:

$$-Li_2(-y) \rightarrow \frac{1}{2}\log^2(y) + \frac{\pi^2}{6}$$

which follows from the following known functional identity[180], as $Li_2(y^{-1}) \rightarrow 0$ while y tends towards ∞

$$-Li_2(-y) - Li_2\left(\frac{1}{-y}\right) = \frac{\pi^2}{6} + \frac{1}{2}\log^2(y).$$

By substituting e^x for y we get the approximation for $\mathcal{L}(x)$.

$$\mathcal{L}_2(x) = \frac{1}{2}x^2 + \frac{\pi^2}{6}$$

The derivative of a polylogarithm with index j is equal to the polylogarithm with index $j-1$. The polylogarithm with index $j = 1$ is a variant of the natural logarithm: $Li_1 = -\log(1-x)$.

$$\frac{d}{dx}Li_j(y) = \frac{1}{y}Li_{j-1}(y)$$
$$\frac{d}{dx}Li_2(y) = -\frac{1}{y}\log(1-y)$$

Thus, at the origin, around $x = 0$ and $y = 1$ a series expansion can be made, leading to:

$$-Li_2(y) = \frac{\pi^2}{12} + (y-1)\log(2) + \cdots$$

Finally, as $-x$ tends to ∞ and $y \rightarrow 0$, Li_2 approaches the first element in its series definition (eq A.7) which is simply $y = e^x$ and corresponds to the Boltzmann approximation.

In addition, the asymptotic behavior of the function $\mathcal{H}_2$, defined in eq A.9, is of interest, as it represents the net charge in the graphene sheet $q(p-n)$.

$$\mathcal{H}_2 = \mathcal{L}(-x) - \mathcal{L}(x) \tag{A.9}$$

The asymptotic behavior of $\mathcal{H}_2$ can be easily deduced from $\mathcal{L}$ and is also included in table A.1.

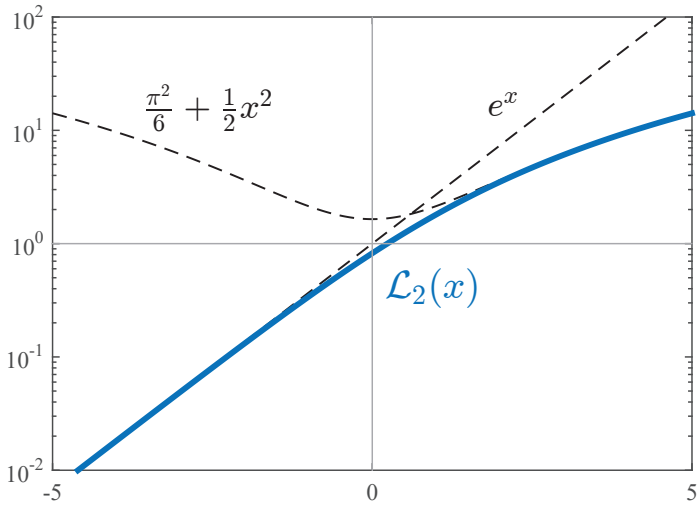


Figure A.1 – Asymptotic approximations of $\mathcal{L}_2(x)$

In region II, it is useful to further simplify the expression by linearizing it:

$$\mathcal{H}_2^0 = (e^{-x} - e^x)\log 2 \tag{A.10}$$

$$= -2\sinh x \log 2 \tag{A.11}$$

$$\mathcal{H}_2^0 \approx -2x\log 2 = -x\log 4 \tag{A.12}$$

It also is of particular interest to know the value of $\mathcal{L}$ at the origin[180]:

$$\mathcal{L}(0) = \frac{\pi^2}{12}. \tag{A.13}$$

Function	Region I	Region II	Region III	
	$\mathbf{x \ll 0}$	$\mathbf{x \approx 0}$	$\mathbf{0 \ll x}$	
	$y \to 0$	$y \approx 1$	$1 \ll y$	
$-\mathbf{Li_2(-y)}$	y	$(y-1)\log(2) + \frac{\pi^2}{12}$	$\frac{1}{2}\log^2(y) + \frac{\pi^2}{6}$	(A.14 a-c)
$\mathcal{L}_\mathbf{2}(\mathbf{x})$	e^x	$(e^x - 1)\log(2) + \frac{\pi^2}{12}$	$\frac{1}{2}x^2 + \frac{\pi^2}{6}$	(A.15 a-c)
$\mathcal{H}_\mathbf{2}(\mathbf{x})$	$\frac{1}{2}x^2 + \frac{\pi^2}{6}$	$(e^{-x} - e^x)\log(2)$	$-\frac{1}{2}x^2 - \frac{\pi^2}{6}$	(A.16 a-c)

Table A.1 – Asymptotic forms of $-Li_2(-y)$, $\mathcal{L}_2(x)$ and $\mathcal{G}(x)$

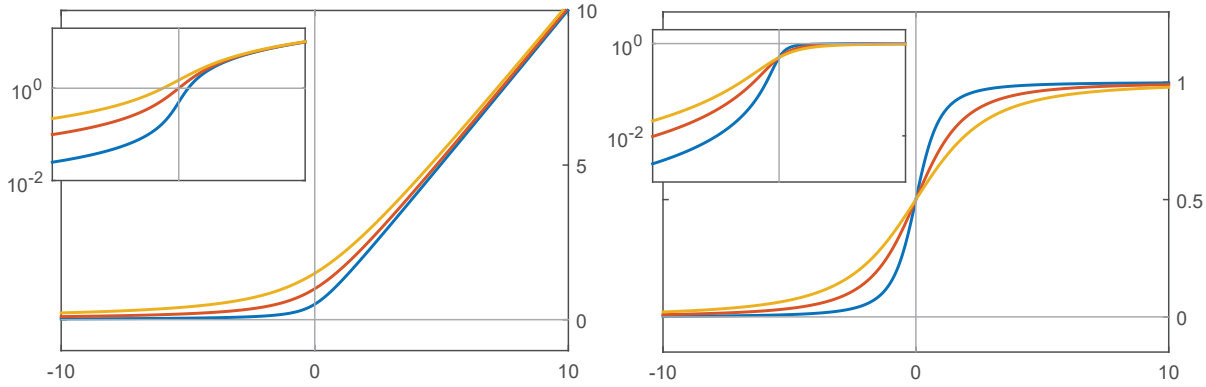


Figure A.2 – Parabolic ramp (a) and step (b) functions plotted for different values of $\alpha = \{1, 2, 3\}$. Insets: linear-logarithmic representation with a horizontal axis identical to the enclosing graph.

A.3 Ramp and Step functions

Ramp and step functions are a versatile mathematical tool that occur and are utilized in several instances throughout this work. The ramp function is first introduced in section 2.4.1, alongside the *V-function* where we discuss elementary curve fitting. The name stems from the appearance of such a function when plotted on a linear scale. In principle, any function $r(x)$ that approaches $r(x) \to 0$ for negative x and $r(x) \to x$ for positive x could be described as a ramp function. The derivative of such a function is called a *step function*. We mostly use the parabolic *ramp* and *step* functions, shown in figure A.2.

$$r(x) = \frac{1}{2}\left(x + \sqrt{\alpha^2 + x^2}\right) \qquad \text{(A.17)} \qquad s(x) = \frac{1}{2}\left(1 + \frac{x}{\sqrt{\alpha^2 + x^2}}\right) \qquad \text{(A.18)}$$

The parabolic ramp function approaches the straight line with slope 1 going through the origin for large, positive x and tends to 0 for large negative x as a hyperbola $\propto 1/x$. The parameter α determines the value at $r(x = 0) = \frac{1}{2}\alpha$ as well as the abruptness of the transition between the left, near-zero and the right, near-linear region. A larger α, leads to a smoother transition but also to higher values in the left-branch.

$$r(x) \to \begin{cases} x & x \gg \alpha \\ \frac{1}{2}\alpha + \frac{1}{2}x + \frac{x^2}{4\alpha} & x \approx 0 \\ \frac{\alpha^2}{4x} & x \ll \alpha \end{cases} \qquad \text{(A.19)}$$

The step function resembles the Heaviside step function with a smooth transition between the left limit 0 and the right limit 1. It approaches 0 faster than $r(x)$ for large negative x proportional to $1/x^2$. The same parameter α in the step function determines the slope at $x = 0$ such that $s'(0) = \frac{1}{2}a$. Again, the larger α, the lower the slope and the less abrupt the transition

between the near-0 and near-1 regions.

$$s(x) \to \begin{cases} 1 & x \gg \alpha \\ \frac{1}{2} + \frac{x}{2\alpha} & x \approx 0 \\ \frac{\alpha^2}{4x^2} & x \ll \alpha \end{cases} \tag{A.20}$$

Both functions can be mirrored across the vertical axis by supplying a negative argument $r(-x), s(-x)$. Also note that the step function is the derivative of the ramp function:

$$\frac{\mathrm{d}}{\mathrm{d}x} r(x) = s(x). \tag{A.21}$$

When integrating a ramp function $r(x)$, the expected result is a base function that resembles $R(x) \sim \frac{1}{2}x^2$ in the right branch, while the left branch should remain close to zero. Without making any assumptions regarding the specific nature of the ramp, one can rewrite the integral by making a change of variable $x \mapsto r$ requiring to divide the integrand by $s(x)$.

$$\int r(x)\,\mathrm{d}x = \int r(x) \left(\frac{\mathrm{d}r}{\mathrm{d}x}\right)^{-1} \mathrm{d}r = \int r(x) \frac{1}{s(x)}\,\mathrm{d}r \tag{A.22}$$

If we multiply the ramp with its derivative, the step functions cancel out and r(x) can be integrated like a polynomial.

$$\int s(x) r(x)\,\mathrm{d}x = \int r(x)\,\mathrm{d}r = \frac{1}{2} r^2(x) \tag{A.23}$$

Note that the product $s(x)r(x)$ is another ramp function. The multiplication with the step function causes it to converge to 0 faster in the left branch but preserves its linear behavior in the right branch where $s(x)$ approaches unity. This is illustrated in figure A.3a where the ramp-step product is plotted next to the original ramp function for comparison. Only in the vicinity of the origin, where $s(0) = 1/2$, does multiplication with the step function alter the result significantly. Since the ramp parameter α directly determines the value of $r(0)$, an adjustment $\hat{\alpha} = 2\alpha$ can be made to ensure $r(0) = \hat{s}(0)\hat{r}(0)$, where $\hat{s}, \hat{r}$ are the ramp and step functions having the adjusted ramp parameter $\hat{\alpha}$. This so adjusted ramp-step product is also plotted figure A.3a.

The base function of $\hat{s}(x)\hat{r}(x)$ is practically equal to the integral of $r(x)$ for positive x and in the vicinity of the origin and differs only in the rate at which it converges to zero in the left branch. Therefore one can state that integrating $r(x)$, as a very good approximation, amounts to taking its square (multiplied by 1/2) while making the appropriate ramp parameter adjustment:

$$\int r(x)\,\mathrm{d}x \approx \frac{1}{2} \hat{r}^2(x) \tag{A.24}$$

This could be referred to as a *polynomial* ramp integral. Figure A.3b shows this integral with

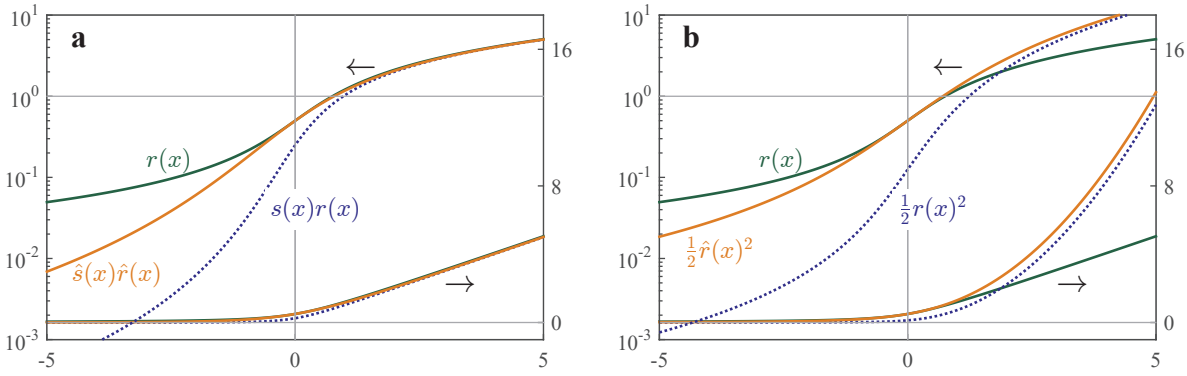


Figure A.3 – (a): Plot of a parabolic ramp function r and the same ramp function multiplied by its step function s. In one case with adjusted ramp parameter α: $(\hat{r}, \hat{s})$ and in the other case without. (b): Ramp function $r(x)$ and its

and without ramp-parameter adjustment.

To understand the role of the step function in this context, it is useful to discuss the asymptotic behavior of the ramp function and its variants. The decay of r is proportional to $1/x$ and that of s is $1/x^2$, therefore the product $s \cdot r$ decays as $1/x^3$. Integration has the property of enhancing growth rate and alleviating decay. The parabolic ramp function's antiderivative has a decay proportional to $\log|1/x|$, which is problematic since it does not converge to a asymptotic limit and is therefore **not** a ramp function. The integral $\int s \cdot r = r^2$ on the other hand has a $1/x^2$ decay; this is another reason why the parabolic integration is preferred here.

In this sense, one could define a sequence of ramp functions, so to say a poly-ramp function, where each element $R_k(x)$ is the polynomial integral of the preceding element $R_{k-1}(x)$:

$$R_k(x) = \frac{1}{k!} r_k(x)^k \tag{A.25}$$

with the property

$$R_k(x) = \int s_k(x) \frac{1}{(k-1)!} r_k(x)^{k-1} \, \mathrm{d}x \tag{A.26}$$

where r_k is the usual parabolic ramp function with parameter α_k

$$r_k(x) = \frac{1}{2}\left(x + \sqrt{\alpha_k^2 + x^2}\right) \tag{A.27}$$

and s_k the associated step function

$$s_k(x) = \frac{\mathrm{d}r_k}{\mathrm{d}x} = \frac{1}{2}\left(1 + \frac{x}{\sqrt{\alpha_k^2 + x^2}}\right) \tag{A.28}$$

The main criterion is that the value at $x = 0$ must be equal in subsequent r_k

$$\frac{1}{k!} r_k(0)^k = s_{k+1}(0) \frac{1}{k!} r_{k+1}(0)^k \tag{A.29}$$

leading to

$$\alpha_{k+1} = \sqrt[k]{2}\, \alpha_k \tag{A.30}$$

This shows that the here described parabolic ramp function can be indefinitely integrated by polynomial integration and represent quadratic ramps, cubic ramps or ramps of any higher degree.

Another example of a ramp function is the exponential ramp function

$$r_{\exp}(x) = \log(1 + e^x) \tag{A.31}$$

which, contrarily to the parabolic ramp function, exhibits exponential rather than hyperbolic decay in the left branch. The exponential ramp function is identical to $\mathcal{L}_1(x) = -Li_1(-e^x)$. Its derivative is known as the logistic function

$$s_{\exp}(x) = \frac{1}{1 + e^{-x}}. \tag{A.32}$$

and the higher order $\mathcal{L}_k$ functions behave much like the parabolic poly-ramp function defined above, and could be referred to as the exponential poly-ramp function.

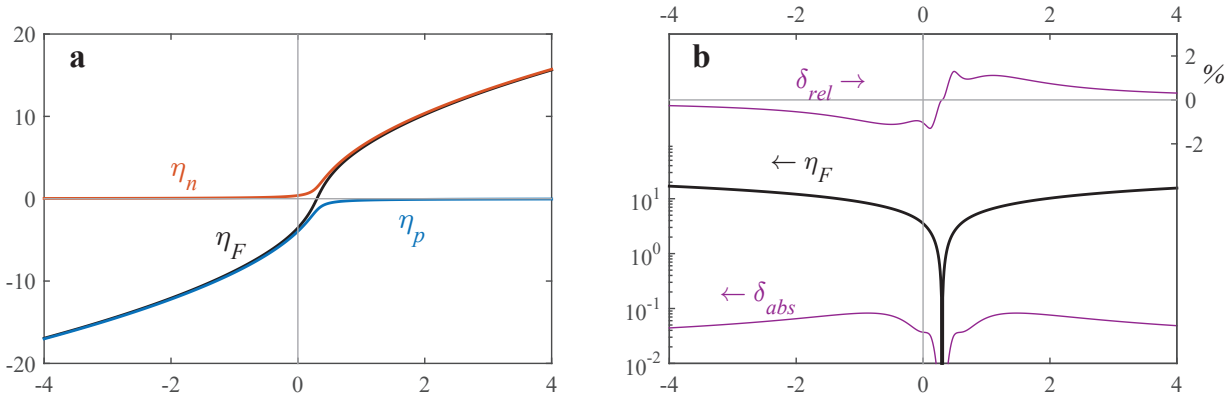


Figure A.4 – Approximation of η_F as a function of voltage using ramp functions substituted in the reduced segment-wise solutions of the charge-voltage relation (a). Absolute and relative error compared to the numerical solution of η_F (b).

A.4 Carrier Concentration modeling using ramp and step functions

Ramp functions are particularly useful when square-root expressions limit the domain of a function to only positive values. This is the case for example in the segment-wise solutions (4.20) to the charge voltage relation (4.17). By replacing $b = b'v$ with $b'r(v)$ and $-b$ with $b'r(-v)$ we can express η_F using the reduced solutions of regions I and III:

$$\tilde{\eta}_F(v) = \sqrt{a^2 + 2b'r(v)} - \sqrt{a^2 + 2b'r(-v)} \tag{A.33}$$

Finally this approach allows to formulate a closed-form approximation of $(\mathcal{L} \circ \eta_F)(v)$, by plugging (A.33) into (A.8), resulting in equations (A.34) below. On a graph, the curves of the exact (numerically solved) solution and the approximation using the ramp function are indistinguishable. Instead, the absolute and relative errors are presented in figure A.4.

$$n(v) = N_G \mathcal{L}_2(+\tilde{\eta}_F(v)) \qquad p(v) = N_G \mathcal{L}_2(-\tilde{\eta}_F(v)) \tag{A.34 a,b}$$

The value of the ramp parameter α, is chosen such that the derivative at $v = 0$ of (A.33) is identical to the slope of η_F (4.20b), which has the value $b'/(a + \log 4)$ in that point. Note that the value of (4.20b) and its derivative at $v = 0$ are exact.

$$\alpha = \frac{1}{b'}\left((a + \log 4)^2 - a^2\right) \tag{A.35}$$

While equation (A.34) provides a convenient and accurate representation of the carrier concentrations, it cannot be integrated to a closed-form expression and provides little insight into the nature of carrier concentrations and the current flowing in the transistor from an algebraic point of view.

If we substitute the (reduced) asymptotic solutions (4.19) for η_F of the charge-volgate relation (4.10) back into the asymptotic forms (A.15) of $\mathcal{L}(\eta_F)$ for the corresponding regions, we obtain the results presented in table A.2. The following considerations are made with regard to electrons while for holes Region I and Region III are interchanged.

Region I: $\mathcal{L}_2(x)$ for large, negative x, behaves like an exponential. We use the reduced solution of $\tilde{\eta}_F$, obtained from the parabolic approximation of $\mathcal{H}_2(x)$, which is essentially a square-root in terms of v. This is the *minority branch* of the electron concentration.

Region II: Around zero, we use the linearized approximations for $\mathcal{L}_2$ and $\mathcal{H}_2$. Although this does not lead to a very faithful representation of the actual shape of $\mathcal{L}_2(\eta_F)$, the values at $v = 0$ and its derivative, which are most important, are exact. This is the *transition branch* of the carrier concentrations.

Region III: Here, the solution of the parabolic equation, is substituted back into the parabolic approxmation of $\mathcal{L}_2$. In terms of v this results in a first-order term b and a square-root term $a^2 - a\sqrt{a^2+2b}$. Note that the square-root term is zero for $b = 0$. This is the *majority branch* of the electron concentration.

	Region I	Region II	Region III	
	$x \ll 0$	$x \approx 0$	$x \gg 0$	
$\mathcal{L}_2(x)$	e^x	$x\log 2 + \frac{\pi^2}{12}$	$\frac{1}{2}x^2 + \frac{\pi^2}{6}$	
η_F	$a - \sqrt{a^2-2b}$	$\frac{b}{a+\log 4}$	$-a + \sqrt{a^2+2b}$	
$\mathcal{L}_2(\eta_F)$	$e^{a-\sqrt{a^2-2b}}$	$\frac{b\log 2}{a+\log 4} + \frac{\pi^2}{12}$	$b + a^2 - a\sqrt{a^2+2b}$	(A.36 a-c)
$\mathcal{L}_2(-\eta_F)$	$b + a^2 - a\sqrt{a^2-2b}$	$\frac{-b\log 2}{a+\log 4} + \frac{\pi^2}{12}$	$e^{-a+\sqrt{a^2+2b}}$	(A.37 a-c)

Table A.2 – Substituting the reduced solutions of the equation $\mathcal{H}_2(x) = ax - b$ into $\mathcal{L}(x)$.

The expressions resulting from the substitutions are particularly relevant in region III for $\mathcal{L}(\eta_F)$ (electrons) and in region I for $\mathcal{L}(-\eta_F)$ (holes), where they represent the normalized carrier concentrations for the majority carrier type of the respective region. Due to the squre-root terms the expressions are valid only within the region where they are defined and assume complex values elsewhere. They can, however, be extended to not only be valid over the full range of v but also present an accurate representation for the carrier concentrations in all

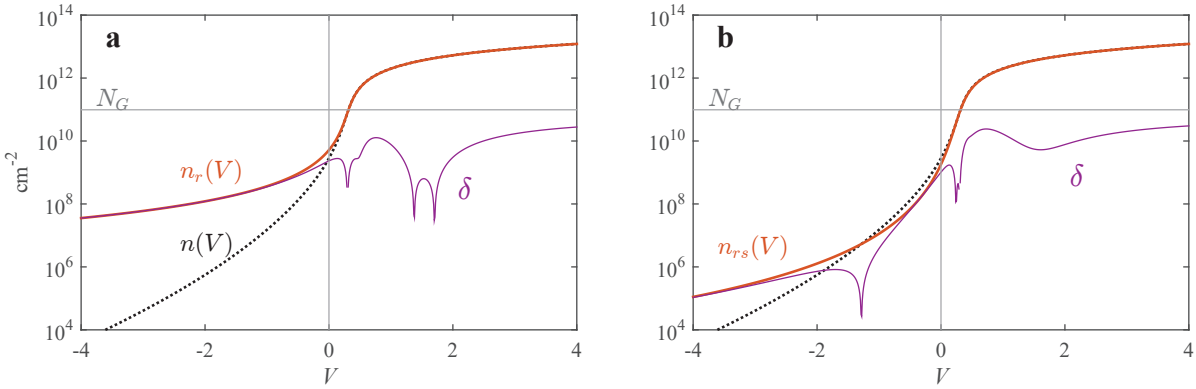


Figure A.5 – (a) Normalized electron concentration n approximated using the majority carrier extended asymptotic solution n_r (A.38), (b) enhanced in the minority carrier branch n_{rs} through multiplication with the step function (A.18).

regions. Like before, we replace $\pm b$ with the corresponding parabolic ramp function $b'(\pm v)$:

$$n_r(v) = N_G \frac{1}{2}\left(-a + \sqrt{a^2 + 2b'r(v)}\right)^2 \tag{A.38a}$$

$$p_r(v) = N_G \frac{1}{2}\left(a - \sqrt{a^2 + 2b'r(-v)}\right)^2 \tag{A.38b}$$

The ramp parameter α is chosen such as to force the function to the exact value at $v = 0$, $n_r(0) = p_r(0) = N_G\mathcal{L}_2(0) = \frac{\pi^2}{12}N_G$:

$$\alpha = \frac{\left(a + \frac{\pi}{\sqrt{6}}\right)^2 - a^2}{b'} \tag{A.39}$$

The result can be seen in figure A.5a. The region-wise solutions (A.36c) and (A.37a) are 0 for $b = 0$ and the ramp function $r(v)$ also approaches 0 fast for negative v. Because of this, the ramp-extended parabolic solutions (A.38), $n_r(v)$, $p_r(v)$, also tend to 0 in their respective minority branch region. On a linear-scale plot the curves are indistinguishable from the numerically computed carrier densities. On a log-scale plot however, as in figure A.5, a gap in the minority branch region becomes apparent that grows increasingly large as $|v|$ increases. This is because the exact n, p exhibit an exponential decay while n_r, p_r follow a hyperbolic decay. The absolute error is nonetheless very small and, considering that in the corresponding region, the total carrier concentration will be dominated by the respective *other* carrier type, is acceptable for the present intents and purposes.

The fidelity can be further improved by multiplying (A.38) with the step function (A.18), forcing the minority branch even closer to zero as can be seen in figure A.5. The ramp parameter α

has to be adjusted in this case and becomes:

$$\alpha = \frac{\left(a + \frac{\pi}{\sqrt{3}}\right)^2 - a^2}{b'} \tag{A.40}$$

Multiplying with the step function also facilitates integration as has been discussed in section A.3.

A.5 Current evaluation based on η_F

Current can be evaluated based directly on the original expression of carrier concentration $n, p = \mathcal{L}_2(\pm\eta_F)$ via integration by $\mathrm{d}v$. This is, in fact, the more rigorous approach also taken in reference [172]:

$$I_{n,p} \propto \int \mathcal{L}_2(\pm\eta_F)\,\mathrm{d}v \tag{A.41}$$

In order to solve this integral we need to make a change of variable $v \mapsto \eta_F$. This can be achieved by taking the derivative of the charge-voltage relation (4.17):

$$\frac{\mathrm{d}}{\mathrm{d}\eta_F}\mathcal{H}_2(\eta_F) = \frac{\mathrm{d}}{\mathrm{d}\eta_F}\left(a\eta_F - b\right) \tag{A.42}$$

which leads to

$$\mathcal{H}_1(\eta_F) = a - b'\frac{\mathrm{d}v}{\mathrm{d}\eta_F}, \tag{A.43}$$

where $\mathcal{H}_1(x) = \mathcal{L}_1(x) + \mathcal{L}_1(-x)$ is the derivative of $\mathcal{H}_2$. After some manipulation, knowing that $a/b' = 1$ one obtains

$$\mathrm{d}v = \left(1 - \frac{1}{b'}\mathcal{H}_1(\eta_F)\right)\mathrm{d}\eta_F. \tag{A.44}$$

The integral can now be rewritten as

$$\int \mathcal{L}_2(\eta_F)\,\mathrm{d}v = \int \mathcal{L}_2(\eta_F)\left(1 - \frac{1}{b'}\mathcal{H}_1(\eta_F)\right)\mathrm{d}\eta_F \tag{A.45}$$

which consists of one simple term and one composite term. The former is very straightforward to evaluate

$$\int \mathcal{L}_2(\eta_F)\,\mathrm{d}\eta_F = \mathcal{L}_3(\eta_F) \tag{A.46}$$

while the latter can be solved through integration by parts, knowing that $\mathcal{L}_1(x) - \mathcal{L}_1(x) = x$ and $\mathcal{L}_0(x) + \mathcal{L}_0(-x) = 1\ \forall x$.

$$\int \mathcal{L}_2(\eta_F)\mathcal{H}_1(\eta_F)\,\mathrm{d}\eta_F = \mathcal{L}_2(\eta_F)^2 - \eta_F\mathcal{L}_3(\eta_F) + \mathcal{L}_4(\eta_F) \tag{A.47}$$

The complete integral is thus

$$\int \mathcal{L}_2(\eta_F)\,\mathrm{d}v = \mathcal{L}_3(\eta_F) + \frac{1}{b'}\left(\mathcal{L}_2(\eta_F)^2 - \eta_F\mathcal{L}_3(\eta_F) + \mathcal{L}_4(\eta_F)\right). \tag{A.48}$$

Although the solution comprises $\mathcal{L}$-functions of various orders, it is interesting to note that

Drift Current		
rigorous approach	pseudo-Fermi level	reference polynomial
$\frac{1}{b'}\left(\mathcal{L}_2(\eta_F)^2 - \eta_F\mathcal{L}_3(\eta_F) + \mathcal{L}_4(\eta_F)\right)$	$\frac{1}{8b'}\eta_n^4$	$\frac{x^4}{4!} = \frac{x^4}{24}$
Diffusion Current		
$\mathcal{L}_3(\eta_F)$	$\frac{1}{6}\eta_n^3$	$\frac{x^3}{3!} = \frac{x^3}{6}$

Table A.3 – Comparison of 3rd and 4th order terms corresponding to electron diffusion and drift current, respectively, as obtained by integration of the η_F (left column) and η_n (center column) -based expressions for carrier concentration. The right column provides a standard polynomial for reference.

all three terms in (A.47) have a 4th-order polynomial character, while (A.46) obviously has 3rd order behavior in the polynomial branch. Comparing equations (A.46)–(A.48) with the definitions of the current components in section 4.5, it becomes clear that (A.46) and (A.47) represent diffusion and drift current respectively. In fact, equations (A.46)–(A.48) quite directly correspond to (4.41)–(4.43) in section 4.5.3. A comparison of the relevant terms is given in table A.3 illustrates the resemblance.

The coefficient $1/6$ in the diffusion term is straightforward, and naturally comes with twofold integration as illustrated by the reference polynomial. In the drift term, a factor $1/b'$ is consistently present but the expected coefficient of a generic 4th order term is $1/24$ contrasting with the coefficient of $1/8$ in the center column. However, since there are, in fact, three 4th order terms in the left column, the coefficient can be explained with a multiplication by $3 \times 1/24 = 1/8$. This considerations confirm that there is a strong qualitative equivalence in the two integration approaches based on η_F and on $\eta_{n,p}$.

We can use this equivalence to cross-check the results obtained in section 4.5.3 and to evaluate the quantitative error induced by the approximations that were made. By solving the charge-voltage relation (4.17) numerically for η_F and plugging the result into (A.48) we obtain an exact reference against which to compare our model. We can also use (A.46) and (A.47) to evaluated at $\eta_F = 0$ in order to determine the appropriate ramp parameter for the parabolic ramp approximation of b_n and b_p.

Equating $\mathcal{L}_k(\eta_F) = \eta_n^k/k!$ at the origin where both v and η_F are zero,

$$\mathcal{L}_k(0) = \frac{1}{k!}\left(a - \sqrt{a^2 + 2b'r(0)}\right)^k \tag{A.49}$$

given that $r(0) = \frac{1}{2}\alpha$ leads to

$$\alpha = \frac{1}{b'}\left(\left(a + \sqrt[k]{k!\mathcal{L}_k(0)}\right)^2 - a^2\right) \tag{A.50}$$

where $\mathcal{L}_k(0)$ can be evaluated using the Riemann zeta function $\mathcal{L}_k(0) = \left(1-2^{1-k}\right)\zeta(k)$. For the ramp adjustment of for the more intricate expression (A.47) we have

$$\left(\mathcal{L}_2(\eta_F)^2 - \eta_F\mathcal{L}_3(\eta_F) + \mathcal{L}_4(\eta_F)\right)\Big|_{\eta_F=0} = \frac{\pi^4}{60} \tag{A.51}$$

thus the corresponding ramp parameter is

$$\alpha = \frac{1}{b'}\left(\left(a + \sqrt[4]{\pi^2/15}\right)^2 - a^2\right). \tag{A.52}$$

The adjusted ramp parameter helps mitigate numerical error at and in the vicinity of the Dirac point in particular.

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